WELCOME FROM THE GENERAL CHAIR

General Chair

Dina Triyoso
General Chair

Kirsten Moselund
Technical Program

Jan Hoentschel
Technical Program
Vice Chair

On behalf of the entire IEDM committee, it is my absolute pleasure to welcome you to the 2023 IEDM in San Francisco from December 9-13, 2023. I am pleased to state that the conference continues its long tradition as the world's premier venue for presenting the latest breakthroughs in semiconductor technologies and devices, as shown in our promotional video at IEDM 2023 video. As every year, IEDM 2023 will feature outstanding contributed and invited papers from industrial and academic leaders as well as students from around the world. An outline of the technical program and short summaries of all the papers are available on the IEDM website– http://www.ieee-iedm.org/. The electronic digest will also be available through IEEE Xplore after the conference.

The meeting kicks off on Saturday, December 9, with our popular and highly successful tutorials. Now in their 13th year, they are targeted at students, practitioners or anyone who is looking for the connection between text-book level knowledge and leading-edge current research. The topics for 2023 are: **"Innovative Technology for Beyond 2 nm", "CMOS+X: Functional Augmentation of CMOS for Next-Generation Electronics", "Reliability Challenges of Emerging FET Devices", "Advanced Packaging and Heterogeneous Integration - Past, Present & Future", "Synapses, Circuits, and Architectures for Analog In-Memory Computing-Based Deep Neural Network Inference Hardware Acceleration", "Tools for Device Modeling: From SPICE to Scientific Machine Learning".** On Sunday, two comprehensive short courses will be offered: **"Transistor, Interconnect, and Chiplets for Next-Generation Low-Power & High-Performance Computing"**, and **"The Future of Memory Technologies for High-Performance Memory and Computing"**. The short courses are organized and presented by internationally recognized researchers and technologists from industry and academia active in these areas. The topics and instructors have been carefully chosen to have broad appeal to IEDM participants and will include material suitable for both newcomers and experts.

The main conference will open with the Plenary Session on Monday morning with three featured talks. First, Siyoung Choi from Samsung Foundry Business will talk about **"Redefining Innovation: A Journey forward in the New Dimension Era"**, followed by Thy Tran from Micron who will address **"Making Memory Magic and the Economics Beyond Moore' Law"**, and finally Björn Ekelund from Ericsson who will talk about **"Semiconductor Challenges in the 5G and 6G Technology Platforms".**

In addition to the excellent contributed paper sessions, four special Focus Sessions will feature talks from leading experts in exciting new and rapidly advancing areas. The topics are **3D Stacking for Next-Generation Logic & Memory by Wafer Bonding and Related Technologies, Logic, Package and System Technologies for Future Generative AI, Neuromorphic Computing for Smart Sensors and Sustainability in Semiconductor Device Technology and Manufacturing**.

On Tuesday evening, we will feature an interactive panel session on **"AI: Semiconductor Catalyst? Or Disrupter?", which** will bring together industry experts to have a conversation on how AI is changing the semiconductor industry and to ask them how they are using AI to transform their efforts. On Tuesday, we present the entertaining **IEDM Career Luncheon at 12:20 p.m.**. Isabelle Ferain from GlobalFoundries and Ilesanmi Adesida from Nazarbayev University, Kazakhstan will share their personal perspectives and their career paths in the semiconductor industries and academia, in an interactive session with a focus on students and young professionals. The discussion will be moderated by Jennifer Zhao from asm OSRAM USA Inc

IEDM 2023 will host an Exhibits section where you can look around and learn more about the latest products and publications. Stop by any time during the exhibition open hours to browse the booths and interact with the participating vendors.

I want to express my sincere appreciation to all authors and speakers who contributed to the technical program. Your efforts are the engine that continues to make IEDM the premier conference in electron devices and related technologies. I also wish to thank each of the members of the IEDM executive and technical subcommittees whose dedication and effort were critical in planning and organizing the 2023 conference.

IEDM is sponsored by the IEEE Electron Devices Society. If you are not already an IEEE and EDS member, please consider joining this great institution that has played such an important role globally for over 130 years. More detailed information regarding the IEEE is available at the conference and on their website – http://www.ieee.org.

It is my great honor and pleasure to extend a warm welcome to everyone attending the 2023 IEEE International Electron Devices Meeting from around the world.

Dina Triyoso

Executive Committee

Front row left to right: Jungwoo Joh, Publicity Chair; Srabanti Chowdhury, Focus Session Co-Chair; Jean Anne Incorvia, Courses Chair (Tutorials); Kirsten Moselund, Technical Program Chair; Dina Triyoso, General Chair; Jan Hoentschel, Technical Program Vice-Chair; Sandy Liao, Asian Arrangement Chair; Shawn Boon, Conference Manager

Second row left to right: Gaudenzio Meneghesso, Courses Chair; Kirsten Weide-Zaage, European Arrangements Chair; Rihito Kuroda, Publications Co-Chair; Marvin Chang, Publications Chair; Hsiang-Lan Lum, MT Chair; Uygar Avci, Virtual Arrangements Chair; Zlatan Stanojevic, MS Chair: Phyllis Mahoney, Conference Manager

Third row left to right: Pei-Jean Liao, RSD Chair; Geert Eneman, Focus Session Chair; Chan Lim, Asian Arrangements Chair; Dechao Guo, Courses Chair (Short Courses); Kang-Ill Seo, Publicity Co-Chair; Lucio Pancheri, ODI Chair

Fourth row left to right: Sangbum Kim, NC Chair; Naomi Yoshida, ALT Chair; Olga Spahn Blum, PMA Chair; Arvind Balijepalli, SMB Chair

Missing: Elena Gnani, EDT Chair; Polly Hocking, Conference Manager; Gail Sparks-Riegel, Conference Manager; John Paul Strachan, European Arrangements Chair

Intro

IEEE International Electron Devices Meeting (IEDM) is the world's preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. IEDM is the flagship conference for nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices and phenomenology, optoelectronics, devices for power and energy harvesting, high-speed devices, as well as process technology and device modeling and simulation.

Digital & social media

- LinkedIn: https://www.linkedin.com/groups/7475096/
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- YouTube: https://www.youtube.com/channel/UC9X-8YPHtsy3SMQwU0yZdTg
- Wikipedia: https://en.wikipedia.org/wiki/International_Electron_Devices_Meeting

Topics of Interest

ADVANCED LOGIC TECHNOLOGY (ALT)

Papers are solicited in the areas of CMOS platform technologies and applications (e.g., HPC, LOP, mobile, automotive, low-temperature CMOS, etc.), logic devices and circuits, process integration schemes for advanced nodes, innovations in material, process and metrology techniques, and design technology co-optimization (DTCO) and system technology co-optimization (STCO). Platform technologies include state-of-the-art Si and beyond-Si channel devices, gate-all-around devices, stacked devices with different polarity transistors, advanced interconnect, novel power distribution integration schemes, heterogenous 2.5D/3D integration schemes, and BEOL compatible transistors. Device architecture, device design and analysis, process integration, module advancements in process and patterning, metrology, physical layout effects, techniques for reduced variability, yield, thermal management, methodologies and solutions for DTCO/STCO in the solicited areas are of high interest.

EMERGING DEVICE and COMPUTE TECHNOLOGY (EDT)

Papers are solicited on emerging nano-electronic devices and physics. This includes devices based on novel transport and control mechanisms such as tunnel FET, negative capacitance FET, cold-source FET, topological materials and devices, phase transitions, ferroelectrics and quantum effects. Devices based on low-dimensional systems including 2D materials, CNTs, nanowires, single electron transistors and quantum dots are welcomed. Exploratory devices with novel device functions and/or novel materials for neuromorphic compute, approximate and analog compute, and non-charge-based compute such as spintronics are key topics. Furthermore, emerging state machines and time dynamical compute systems are also of interest. Qubit devices as well as devices and systems designed to enable quantum computing, quantum simulation and quantum annealing are of high interest. Papers in EDT focus primarily on device physics and novel elaboration concepts.

MEMORY TECHNOLOGY (MT)

Papers are solicited in the areas related to embedded and standalone memory technology. This includes advances in both conventional memories including SRAM, DRAM and Flash, and emerging memories including ReRAM, MRAM, PCRAM, ferroelectric memory, crosspoint memory and selectors, organic memory and NEMS-based memory, as well as their applications in the areas of AI and near-Memory compute. Topics span from demonstration of novel device concepts to fully integrated memory arrays, and from product prototyping to manufacturing related challenges and solutions. Demonstrations of manufacturing maturity of emerging memories and future scaling of conventional memories to solve the memory wall issues are of high interest. Submission of papers on novel device concepts and demonstrations, novel integration schemes, novel circuit design schemes, and novel memory architectures that enhance memory performance, scaling, 3D stacking, capacity/bandwidth increasing, and power/energy reduction are strongly encouraged. Papers based on novel device physics and in-memory computing may be transferred to EDT or NC at the discretion of the committee.

MODELING and SIMULATION (MS)

Papers are solicited on theoretical approaches to electronic devices, including logic devices, memory devices, optical devices, interconnects and (bio)sensors. Theoretical approaches include analytical, numerical, statistical, and machine-learning/AI-based approaches applied to structures with dimensions ranging from atomistic over device dimensions to full-chip dimensions, including physics-based compact modeling. Key to submissions is, that the device innovation is central, either through predictive insight in the potential of novel device concepts, predictive analysis revealing significant improvement to devices, breakthroughs in the theoretical understanding of the device operation, breakthroughs in the understanding of device processing enabling improved device performance, novel insights in variability, reliability and yield issues, breakthrough in device optimization based on DTCO. Topics also include ab-initio/atomistic materials modeling, modeling of neuromorphic computing, quantum computing, spintronics, low-dimensional devices, ferroelectrics, thermal modeling, 3D/heterogeneous integration, electro-chemical/mechanical devices. Comparison with experimental data, model calibration and multi-scale simulation chains are highly encouraged.

NEUROMORPHIC COMPUTING (NC):

Papers are solicited in the areas related to devices, circuits, and algorithms for neuromorphic computing and AI. We welcome submissions covering a wide range of areas in neuromorphic computing including but not limited to: analog in-memory deep learning, compute-in-memory, probabilistic/approximate/analog computing, combinatorial optimization, machine learning, and AI applications, edge computing, unclonable functions, reservoir computing, spiking neural network, artificial intelligence, in-sensor computing, and bio-inspired computing based on memory/logic/sensor/nanoelectronic/MEMS devices and their novel architecture and physics. Demonstration of real-world applications, full hardware integration, device-algorithm co-optimization, novel device concepts improving computational efficiency, and new algorithms mitigating non-ideal properties of devices and materials are of high interest.

OPTOELECTRONICS, DISPLAYS, and IMAGING SYSTEMS (ODI)

Papers are solicited on optoelectronics, displays, and imaging systems. This includes novel devices, structures, and integration for image sensors, displays, light sources, photonic devices, and high-speed photodetectors and modulators. New technologies on heterogeneous integration of optoelectronics as well as on photonic-electronic integration for optical interconnects, on-chip networks and sensing are welcomed. Papers on quantum photonics, neuromorphic photonics, and plasmonics for quantum computation, sensing and encryption are also of interest. Furthermore, ODI includes CMOS imagers, high-speed and high-time resolution imagers, CCDs, stacked, single-photon and non-visible image sensors. In addition, papers on displays for augmented or virtual reality, holography, TFTs for photonics applications, flexible, stretchable, and/or printed electronics, in-display sensors are encouraged. Papers on displays or light emitting devices with novel materials such as perovskites or quantum dots are also of interest. We particularly welcome submissions concerning optoelectronic or photonic devices or systems based on topological concepts.

POWER, MICROWAVE/MM-WAVE and ANALOG DEVICES/SYSTEMS(PMA)

Contributions are sought on novel circuit topologies, manufacturing processes, supporting modeling (TCAD and compact models), device physics, reliability, and materials (SiC, (Al)GaN, diamond, Ga2O3, Si, III-Vs, etc.) along with fundamental studies on doping, deep-level traps, interface state densities, and device reliability for power and/or high frequency devices. Papers are solicited on discrete and integrated power and/or high frequency (micro, mm-wave and THz) devices and physics, modules and systems. Topics of interest include devices (diodes, BJTs, FETs, super-junction devices, heterostructures, IGBTs, HEMTs, HBTs, light-triggered structures for galvanic isolation and faster switching, bi-directional switches, vertical geometry devices, etc.) and device/package/circuit interactions, including thermal management. Wide variety of applications are also of interest (power conversion, supply, regulation and conditioning for computers and data centers, motor drives, transportation, solar, wind, smart grid applications, wireless power harvesting/transfer, filters, beam formers, power amplifiers, tunable passives, antenna arrays, SAW/BAW).

RELIABILITY OF SYSTEMS and DEVICES (RSD)

Papers are solicited in reliability evaluation (experimental and modeling) of logic and memory devices, interconnects, and circuits and systems, mainly (but not limited) to employing Si-based technologies. Specific reliability topics include, for FEOL: transistor degradation due to hot carriers, bias temperature instabilities, random telegraph noise, and aging model; dielectric SILC and wear-out. For MEOL/BEOL, topics include breakdown of MEOL spacers and BEOL dielectrics; electromigration, stress migration failures of contacts and interconnects. For product, system, and circuit reliability, topics include latch-up, ESD, soft error mechanisms, variability-aware design, and design for reliability, robustness, and security of electronic circuits and systems. Of particular interest are investigations of degradation mechanisms for devices, circuits, and systems in the following areas: conventional and emerging memories; beyond CMOS devices; 3D IC package reliability, more-than-Moore applications; biomedical devices and systems; automotive and aerospace.

SENSORS, MEMS, and BIOELECTRONICS (SMB)

Papers are solicited in the areas of sensors, micro/nano electromechanical systems (MEMS and NEMS), microfluidics/lab-on-chip, and BioMEMS, with particular emphasis on new device concepts, integrated and highly parallel CMOS implementations, CMOS-on-MEMS, embedded machine learning, organic-inorganic hybrid microfabrication, flexible devices, and multimodal sensors on a chip for applications in health, medicine, communication, mobility, and energy. Sensors include chemical, molecular and biological detection based on acoustic, electrical, electrochemical, magnetic, mechanical and optical principles. Topics of interest in the MEMS area include actuators, physical and biochemical sensors (BioMEMS), resonators, integrated inertial measurement units, RF MEMS, optomechanical devices, micro-power generators, and devices for energy harvesting as well as on-chip energy storage. Bioelectronics covers organic-inorganic hybrid devices, point-of-care biomedical devices, bio-electronic interfaces, integrated biomedical sensing, and implantable sensors and neural interfaces.

Program

Tutorials

The tutorials are in their fourteenth year and are standalone presentations on specialized topics taught by world-class experts. These tutorials will provide a brief introduction to their respective fields and facilitate understanding of the technical sessions. In contrast, the traditional short courses are focused on a single technical topic.

All Tutorials will be held on Saturday, December 9, 2023.

Tutorials
Saturday, Dec. 9
Co-Chairs: Jean Anne Incorvia, University of Texas Austin
Dechao Guo, IBM and Gaudenzio Meneghesso, University of Padova
1:30 PM - 6:00 PM

Tutorial 1: Innovative Technology for Beyond 2 nm, Matthew Metz, Intel Corp.
1:30 PM– 2:50 PM
Continental 4-5
Chair: Jean Anne Incorvia, University of Texas Austin

Intel is working at the forefront of revolutionary material and device improvements that the semiconductor industry needs to support continued performance improvements. This tutorial will focus on two of these research topics, Transition Metal Dichalcogenides for continued CMOS scaling and new materials and devices for ultra-low power computation.

Tutorial 2: CMOS+X: Functional Augmentation of CMOS for Next Generation Electronics, Sayeef Salahuddin, University of California, Berkeley

1:30 PM – 2:50 PM
Continental 6-9
Chair: Dechao Guo, IBM

Despite ominous foretelling of a slowdown, over the last decade the computational throughput has increased by orders of magnitude. Energy efficiency is critical not only to maintain this incessant advancement, but also to ensure that electronics does not become a drag on the finite energy resources of the world. This will need a radical rethinking of the basic building blocks that constitute the electronic hardware. In this talk, I shall briefly present how integrated ferroelectric devices offer a new pathway in this context. First, I shall discuss the phenomenon of negative capacitance in ferroelectric materials. A fundamentally new state in the ferroelectric materials, negative capacitance promises to reduce power consumption in electronic devices significantly. I shall discuss our current understanding of negative capacitance derived from numerous experimental works done over the last few years. We shall further discuss the material science that is enabling the integration of negative capacitance into advanced transistors. Going beyond transistors, the insight gained from physics and materials could also lead to advanced, low power memory devices. Additionally, I shall present integrated magnetic devices. Beyond memory applications, these devices are showing promise for neuromorphic computing and sensing applications. These examples underscore how functional augmentation of CMOS by harnessing new physical phenomena, we are calling it CMOS+X, could offer opportunities that are otherwise not available through conventional means.

Tutorial 3: Reliability Challenges of Emerging FET Devices, Jacopo Franco, imec
3:05 PM- 4:25 PM
Continental 4-5
Chair: Jean Anne Incorvia, University of Texas Austin

The unabated performance enhancement of semiconductor technology has been sustained in recent years by disruptive device and material innovations. For the successful deployment of any novel device concept, the promised enhanced performance must be guaranteed for the entire expected lifetime of the final product. Traditionally, device reliability optimization was an aspect considered only at a late stage in the development of a new device technology. We argue that in contemporary devices, fabricated with complex integrations and a plethora of materials, potential reliability issues should be considered from the very early stage of the technology development, as they can potentially disqualify otherwise promising device concepts. In particular, charge trapping in gate dielectrics is an aspect that can “make or break” any MOS-based device, and thus gate stack stability should be considered as a primary metric in the evaluation of novel device concepts. In this Tutorial we will review the fundamentals of charge trapping in gate dielectrics in terms of phenomenology, characterization techniques and physical models. Next, we will briefly discuss as case studies some recent examples of MOS innovations which made it into mainstream technology (e.g., SiGe channels), as well as other examples which to date remain confined to academic research (e.g., III-V and Ge channels for Logic). We will then focus on specific gate stack challenges for upcoming CMOS technology innovations, including Nanosheet and Forksheet device architectures, and novel device concepts such as the stacked Complementary FET (CFET) and 2D channel transistors. To further highlight the general relevance of charge trapping in dielectrics, we will briefly discuss its role also in wide-bandgap semiconductors (GaN, SiC) MOS-based devices for Power and Analog/RF applications. Finally, we will discuss novel transistors based on oxide semiconductor channels (e.g., IGZO), which due to their extremely low off-state leakage and their flexible fabrication flow are considered as potential gamechangers for memory periphery and, in general, for the heterogeneous integration of transistors in the Back End of Line (BEOL). For these devices, we will discuss how the interplay between their gate dielectric and channel instabilities makes the reliability assessment and optimization particularly complex and requiring the combination of electrical and optical characterization techniques.
3:05 PM

Tutorial 4: Advanced Packaging and Heterogeneous Integration - Past, Present & Future, Madhavan Swaminathan, Penn State
3:05 PM – 4:25 PM
Continental 6-9

Chair: Gaudenzio Meneghesso, University of Padova

The global semiconductor industry is projected to become a trillion-dollar industry by 2030. This is historic considering that it took the industry 55 years to reach half a trillion dollars in size and will take just another 10 years to double in size to a trillion dollars. Advanced packaging as it relates to heterogeneous integration will play an important role in making this happen. This tutorial will cover the fundamentals of advanced packaging covering the past and present state of the art including what is necessary in the future to enable heterogeneous integration. Metrics used to compare these technologies will be discussed.

Tutorial 5: Synapses, Circuits, and Architectures for Analog In-Memory Computing-Based Deep Neural Network Inference Hardware Acceleration Irem Boybat, IBM Research Europe
4:40 PM – 6:00 PM
Continental 4-5
Chair: Jean Anne Incorvia, University of Texas Austin

The advent of deep neural networks (DNNs) has revolutionized numerous fields, including computer vision and natural language processing. These powerful models have showcased remarkable capabilities in solving complex problems, but their training and inference procedures often require significant computational resources. To address this challenge, notable activity was centered around specializing or developing digital hardware accelerators for DNNs, such as graphics processing units (GPUs) and tensor processing units (TPUs). However, this talk will go beyond digital acceleration and instead focus on the emerging field of analog in-memory computing (AIMC). More specifically, it will delve into devices, synapses, circuits, and architectures for building energy efficient yet accurate AIMC-based accelerators for DNNs. We will explore how the AIMC paradigm can overcome the limitations of traditional digital computing approaches and offer better energy efficiency by blurring the distinction between memory and computing. We will investigate the impact of device characteristics and their organization into synapses on DNN inference and training accuracies. Furthermore, we will discuss the role of peripheral circuits and accelerator architectures on energy efficiency and performance.

Tutorial 6: Tools for Device Modeling: From SPICE to Scientific Machine Learning, Keno Fischer, JuliaHub, Inc.
4:40 PM - 6:00 PM
Continental 6-9
Chair: Gaudenzio Meneghesso, University of Padova

How do we know if our devices will work before we tape them out? Since the dawn of the semiconductor industry, modeling and simulation has been a cornerstone of both process development and pre-tapeout verification. And yet, despite this rich heritage, some of the most impactful capabilities remain underutilized or locked away in hard-to-use, bespoke tools. In this tutorial, we will take a look at the modeling modalities available for semiconductor devices, from our venerable compact MOSFET models, through TCAD, down to direct Density Functional Theory calculations. We will explore how we can leverage these models beyond simple simulation for device optimization, characterization, model calibration and more. Then, we will turn to more recent techniques, exploring how Scientific Machine Learning allows the creation of multi-scale surrogate models at tunable fidelity and performance. Finally, we will look at our real-world experiences developing CedarEDA and vision for the future of device modeling and how we can bring advanced modeling closer to engineering practice to reduce the costly iterations, build better devices, and improve our engineering productivity.

Short Courses

IEEE IEDM will offer two short courses with in-depth coverage of highly relevant topics from world experts. All short courses will be held on Sunday, December 10.

Sunday, Dec. 10

Short Course 1: Transistor, Interconnect, and Chiplets for the Next Generations of Low-Power & High-Performance Computing
9:00 AM, Continental 4-5
Co-Chairs: Yuri Masuoka, Samsung and Dechao Guo, IBM
9:00 AM

1-1 Advanced Technology Requirement for Edge Computing, Jie Deng, Qualcomm
The next-generation computing market is poised to experience an astounding six-fold surge from 2023 to 2033, driven by a remarkable compound annual growth rate (CAGR) exceeding 19% in the next decade. The escalating computing demand intensifies the necessity for optimal low-power and high-performance solutions. Achieving continuous power-performance scaling demands seamless synergy between transistors, interconnects, and packaging technologies. With FinFET scaling approaching its limits, innovative device architectures emerge as promising candidates for next-generation transistor technology, including gate-all-around (GAA/NS), Forksheet FET (FS), complementary FET (CFET), 2D-material FET. To address large wire delay and the high IR drop issue resulting from continuous area scaling, novel interconnect material and innovative integration schemes like Backside Power Delivery (BSP) are required. Furthermore, the semiconductor industry is moving towards advanced heterogeneous packaging platforms for both 2.5D and 3D integration. In this short course, we will explore the current state of transistor, interconnect, and packaging technologies, review challenges in continuous power-performance scaling, and delve into emerging technologies for next-generation low-power, high-performance computing. Additionally, we will discuss economic impact and production interception timeline outlook of various emerging technologies for different applications.

10:40 AM
1-2 Process Technology Towards 1nm and Beyond, Tomonari Yamamoto, [1]TEL
This short course will cover the processes technologies that enable the continuous evolution of logic transistors and interconnects towards the 1nm node and beyond. The critical metric for logic density is the product of the "logic cell width x logic cell height". Gate pitch scaling is a crucial factor for scaling logic cell width. To enable this, scaling of gate length, gate spacer width, and contact feature size is necessary. Gate-All-Around (GAA) technology improves electrostatics compared to FinFETs and enables continuous gate length scaling. Material advancements are necessary to mitigate parasitic capacitance and resistance increase while securing yield and reliability of the transistors. In terms of the logic cell height, advancements in layout and transistor structure innovations, as well as interconnect metal pitch scaling, contribute to its scaling. Continuous RC reduction techniques have been implemented for copper interconnect extension with metal pitch scaling. Eventually, alternative metals that outperform copper in CD sizes of 10nm and below need to be considered. Regarding layout and transistor structure innovations, a backside Power Delivery Network (PDN) is an attractive option for better area utilization and performance enhancement. Additionally, Complementary FET (CFET), which consists of stacked transistors, is a promising architecture for enabling continuous logic cell height scaling. To enable these advancements, continuous process and tool advancements are necessary not only in film, etch, lithography, and wet processing but also in wafer bonding and thinning technologies. The talk will also review recent progress in EUV-related solutions, including self-aligned patterning.

1:10 PM
1-3 Empowering Platform Technology with Future Semiconductor Device Innovation, Jaehun Jeong, [1]Samsung
FinFET, the platform technology in foundry business for more than a decade, has faced fundamental limitations for the further scaling with PPA improvement and it is the time to move on another “New dimension” of transistor. Gate-All-Around (GAA) FETs / MBCFETTM have been already introduced as the logic device for next generation and started mass production. MBCFETTM has been enabling different type of PPA enhancement with the design flexibility allowing additional room for DTCO to optimize standard cell speed/power with various nano-sheet size beyond its intrinsic device gain like short channel effect improvement and high drivability. In the near future, 3D stacked structure connecting multiple layers of transistors vertically and Backside-PDN technology relocating the power delivery network to the backside of the chip will be ready for innovative integration schemes. Also, 2D transistor has been studied to use their high

carrier mobility and excellent electrostatic control enabling another scaling of gate length and pitch. These innovations in the semiconductor industry can bring another breakthrough to enhance the capabilities of foundry platform technologies, and the key to sustainable success lies in how to harness the power of those technological advancement to the platform technology including emerging applications such as mobile SoC, AI, autonomous vehicle and HPC with enhancement of overall chip performance.

2:25 PM

1-4 Future Power Delivery Process Architectures and Their Capability and Impact on Interconnect Scaling, Kevin Fischer, Intel Corporation

As continued semiconductor technology scaling becomes increasingly more challenging and expensive it is crucial to invent ways to enable increasing the ability to interconnect the transistors and slow the degradation of the interconnect properties. Traditionally, degree of connectivity is maintained thru scaling interconnect pitches and feed thru pitches and adding ever more interconnect layers. The cost of this approach is becoming increasingly more impactful we must find new ways to add design value and scaling capability outside of the conventional approach. Novel technologies such as buried power rails can reduce the impact of these effects to a limited extent. One step beyond this lies in the introduction of backside power. Moving power to the backside of the wafer greatly reduces the interconnect tax on the conventional front side interconnects by removing the need spend interconnect resources on power. Beyond backside power advantage lies in leveraging the ability to contact the transistor from top and bottom and introducing dense metal on both frontside and backside. In this short course we will look at the scaling pressures on interconnects driving the need for these new technologies as well as the technologies themselves along with the engineering opportunities and challenges for high volume manufacturing.

4:05 PM

1-5 DTCO/STCO in the Era of Vertical Integration, Y.K. Chong, ARM Ltd.

As we venture into the era of AI, the demand for energy-efficient computation continues to accelerate. However, the relentless push towards smaller semiconductor geometries has brought about significant challenges to technology scaling. To sustain progress, the semiconductor industry must explore alternative approaches. Coordinated innovations across system, circuit, and technology abstraction levels are needed to continue the trajectory of power, performance, area, and cost (PPAC) metrics within compressed product development timelines. In this short course, we offer an industry perspective on the technological and product development challenges of advanced process nodes. We will delve into Design-Technology Co-Optimization (DTCO) and System-Technology Co-Optimization (STCO) strategies that have been explored at Arm, encompassing various techniques applied to logic, SRAM, interconnects, power delivery, system partitioning, and packaging. We hope that our practical insights will help device engineers, circuit designers, and system architects to continue to improve high-performance computing in the sub-3 nm era.

5:20 PM

1-6 Low Power SOC Design Trends/3D Integration/Packaging for Mobile Applications, Milind Shah, Google

Moore's Law has been the driving force behind the scaling of process nodes for decades, enabling higher transistor density in monolithic system-on-chip (SoC) architecture designs. However, cost pressure and longer cycle times for manufacturing monolithic SoC designs in recent process generations have slowed down node scaling, forcing chip designers to explore new architectures to meet higher performance requirements more economically. Chiplet-based architectures with high-density interconnect packaging integration for homogeneous and/or heterogeneous nodes offer a new way to design chips that allow for more flexibility and scalability, as well as the creation of chiplets tailored to specific applications and easier upgrades. This short course will review the current industry landscape of 3D packaging integration solutions, which enable higher off-chip interconnect density, resulting in higher data bandwidth, power efficiency, lower data communication latency and future trends. The broader industry trend of 3D interconnect packaging strategy and optimization will also be highlighted in this study.

Short Course 2: The Future of Memory Technologies for High-Performance Memory and Computing

9:00 AM, Continental 6-9

Co-Chairs: Ki-il Moon, SK Hynix and Gaudenzio Meneghesso, University of Padova

9:00 AM

2-1 High-Density and High-Performance Technologies for Future Memory, Koji Sakui, Unisantis Electronics Singapore/Tokyo Institute of Technology

The agenda is composed of four key technologies: **1) DFM**, **2) KFBM**, **3) SGT**, and **4) BBCube**. 1**) DFM**: A new high-density memory technology called Dynamic Flash Memory (DFM) which can be built using a conventional silicon process. DFM is scalable and has no special material requirements, making it a cost-effective alternative to emerging memory technologies. The proposed stackable DFM eliminates the need for capacitors, resulting in smaller cell sizes than $6F^2$ with 3~4 tiers. **2) KFBM**: A fully CMOS compatible Key shape Floating Body Memory (KFBM) cell consists of MOSFET with virtually floating body formed by bulk silicon and trench with on/off margins of more than three orders of magnitude. The vertical device in KFBM helps to improve retention and disturbance and reduce the scaling pressure. **3) SGT**: A Surrounding Gate Transistor (SGT) has advantages of improved density and reduced power leakage, which means that the SGT is a promising candidate for a switching transistor of a variety of memory devices, such as DRAM. **4) BBCube**: The Bumpless Build Cube (BBCube) 3D has been proposed for AI and HPC applications, which need high bandwidth and power efficiency. The BBCube 3D is constructed by heterogeneous 3D integration in which xPU (CPU, GPU etc.) chips and DRAM wafers are stacked using a combination of bumpless Wafer-on-Wafer and Chip-on-Wafer. The BBCube 3D has the potential to achieve a bandwidth 30 times higher than DDR5 and four times higher than HBM2E with the access energy per bit 1/20th that of DDR5 and 1/5th that of HBM2E.

10:30 AM

2-2 Advanced Packaging Solutions for High Performance Memory and Compute, Jaesik Lee, SK Hynix USA

Generative AI such as ChatGPT and Bard, which are based on large language models capable of producing human like text and images, have becomes mainstream for artificial intelligence technology industries. In order to run the increased model sizes without performance degradation, a large amount of memory needs to be integrated in a system. High bandwidth memory (HBM) is a perfect solution to meet the system requirements like high bandwidth and low power consumption together with concurrent integrations of the logic chips in 2.5D and 3D advanced packaging technologies. 5th generation HBM, HBM3E, has been developed since HBM1 was produced in 2013. The continued scaling of HBM to increase memory capacity and to enhance thermal performance necessitates the evolutions of 3D stacking technologies. In this short course, we will talk on the HBM stacking innovations and their challenges associated with advance packaging technologies. In addition, how to ensure that HBM is compatible to packaging processes and reliability in advanced packaging technologies such as CoWoS-S and CoWoS-L will be presented. HBM challenges associated with system level cooling integration will be also presented.

12:45 PM

2-3 Analog In-Memory Computing for Deep Learning Inference, Abu Sebastian, IBM Research - Zurich

Deep neural networks (DNNs) are revolutionizing the field of artificial intelligence and are key drivers of innovation in device technology and computer architecture. While there has been significant progress in the development of specialized hardware for DNN inference, many of the existing architectures physically split the memory and processing units. This means that DNN models are typically stored in a separate memory location, and that computational tasks require constant shuffling of data between the memory and processing units – a process that slows down computation and limits the maximum achievable energy efficiency. Analog in-memory computing (AIMC) is a promising approach that addressing this challenge by borrowing two key features of how biological neural networks are realized. Synaptic weights are physically localized in nanoscale memory elements and the associated computational operations are performed in the analog/mixed-signal domain.

In the first part of the course, I will introduce AIMC based on non-volatile memory technology. The focus will be on the key concepts and the associated terminology. Subsequently, a multi-tile mixed-signal AIMC chip for deep learning inference will be presented. This chip fabricated in 14nm CMOS technology comprises 64 AIMC cores/tiles based on phase-change memory technology. It will serve as the basis to delve deeper into the device, circuits, architectural and algorithmic aspects of AIMC. Of particular focus will be achieving floating point-equivalent classification accuracy while performing the bulk of computations in the analog domain with

relatively less precision. I will also present an architectural vision for a next generation AIMC chip for DNN inference. I will conclude with an outlook for the future.

2:00 PM
2-4 Key Challenges and Directional Path of Memory Technology for AI and High-Performance Computing, Keith Kim,NVIDIA
AI/ML continues to evolve beyond inferencing and training the image. Especially Generative AI unlocks new possibilities for all industries and larger language model is to accelerate computing resources, driving memory performance and density while focusing on energy efficiency. In addition, security and memory RAS cannot be ignored since data center data integrity is one of key technologies in data center. This short course will address the directional path of memory technology requested by AI/HPC applications, and technical challenges for bandwidth, power, density, RAS, and security. Both barriers and potential technology solutions will be reviewed. Towards resolving memory walls and meeting system requirements, initiatives to develop new memory technologies for AI/HPC are needed.

3:30 PM
2-5 The Next Generation of AI Architectures: The Role of Advanced Packaging Technologies in Enabling Heterogeneous Chiplets, Raja Swaminathan, AMD
As we further race to bring together heterogenous compute and acceleration from the motherboard to the package, our industry will need to solve several new challenges. Chiplet architectures are fundamental to the continued economic viable growth of power efficiency of AI, 5G and edge computing. The slowing of Moore's law has also placed advanced packaging at the critical juncture of technology-architecture intersection driving unique product capabilities. UCIe is a great step forward to address the interconnect aspect, but how do we bring UCIe together with advanced packaging. What standard form factors should we define? How do we enable debug/test beyond KGD? What kind of power delivery and thermal controls will we need? Can we also enable DVFS and binning? How do these challenges differ between advanced and organic packaging solutions? In this course, we will take a look at these questions and discuss some possible ways forward to address these challenges. New heterogeneous architectures like 2.5D Fanout and 3D Hybrid bonded architectures driving AMD's industry leading advanced technology roadmap to enable power, performance, area, and cost (PPAC) as well as challenges and solutions for large chiplet modules etc. will also be discussed.

4:45 PM
2-6 Charge-Trapping Memories: From the Fundamental Device Physics to 3D Memory Architectures (3D NAND, 3D NOR, 3D DRAM) and Computing in Memory (CIM), Hang-Ting (Oliver) Lue, Macronix
Charge-trapping Flash memory devices, including SONOS and its variations, have surpassed floating gate (FG) devices in the commercial market share recently, primarily due to the remarkable success of 3D NAND technology. This concise course will commence with a review of the fundamental physical principles behind bandgap engineered (BE) SONOS, encompassing AB initio modeling of commercially adopted SiON tunnel dielectrics and SiN traps. Detailed scrutiny will extend to 3D NAND architectures, encompassing both standard commercial cells and emerging double-density structures such as hemi-cylindrical or flat cells. Additionally, the potential of 3D NOR structures to offer a superior product performance with low-latency and byte-addressable 3D memory will be explored. Introducing a notable innovation, a micro heater capable of localized heating above 400°C will be presented. This innovation has potential to enhance the P/E cycling endurance of 3D charge-trapping Flash memory to over 100 million cycles, with remarkable high-temperature data retention. Finally, addressing the escalating demands of big-data AI computing, the course will delve into 3D DRAM architectures and the concept of computing in memory (CIM) utilizing 3D memory technology.

Welcome and Awards Presentations

Monday, Dec. 11
Session 1: Welcome and Awards Presentations
Dina Triyoso**,** TEL Technology Center, America, LLC
General Chair
9:00 AM, Grand Ballroom B

2023 IEEE Andrew S. Grove Award

Awarded to Hon-Sum Philip Wong
"For contributions to novel and advanced semiconductor device concepts and their implementation"

2022 Roger A. Haken Best Student Paper Award
Awarded to Ruben Asanovski
For the paper entitled, "New insights on the excess 1/f noise at cryogenic temperatures in 28 nm CMOS and Ge MOSFETs for quantum computing applications"

2022 EDS Paul Rappaport Award
To: Akshay Arabhavi, Filippo Ciabattini, Sara Hamzeloui, Ralf Flückiger, Tamara Saranovac, Daxin Han, Diego Marti, Giorgio Bonomo, Rimjhim Chaudhary, Olivier Ostinelli, and Colombo R. Bolognesi
For the paper entitled: "*InP/GaAsSb Double Heterojunction Bipolar Transistor Emitter-Fin Technology With fMAX = 1.2 THz* "

2022 EDS George Smith Award
To: Sourav De, Franz Müller, Nellie Laleni, Maximilian Lederer, Yannick Raffel, Shaown Mojumder, Alptekin Vardar, Sukhrob Abdulazhanov, Tarek Ali, Stefan Dünkel, Sven Beyer, Konrad Seidel, and Thomas Kämpfe
For the paper entitled: "*Demonstration of Multiply-Accumulate Operation With 28 nm FeFET Crossbar Array*"

2022 EDS Leo Esaki Award
To: Fei Mo, Jiawen Xiang, Xiaoran Mei, Yoshiki Sawabe, Takuya Saraya, Toshiro Hiramoto, Chun-Jung Su, Vita Pi-Ho Hu, and Masaharu Kobayashi
For the paper entitled: "*Efficient Erase Operation by GIDL Current for 3D Structure FeFETs With Gate Stack Engineering and Compact Long-Term Retention Mode*"

2023 EDS Distinguished Service Award
To: Fernando Guarin, Retired, NY, USA
"For Outstanding and Dedicated Service for the Benefit and Advancement of the Electron Devices Society"

2023 EDS Education Award
To: Gary S. May, University of California, Davis, CA, USA
"For dedicated leadership and mentorship that has diversified academic leaders in education"

2023 EDS Lester F. Eastman Award
To: James C. Hwang, Cornell University, Ithaca, NY, USA
"For outstanding achievement in high-performance semiconductor devices"

2023 EDS J.J. Ebers Award
To: Mukta Farooq, IBM, Hopewell Junction, NY, USA
"For development of emerging heterogeneous integration architectures for 3D ICs"

2023 IEEE/EDS Fellows
**This is a complete listing of the 2023 IEEE/EDS Fellows. Not all Fellows will be recognized at the 2023 IEDM*

Shekhar Bhansali - for contributions to portable realtime sensing devices for continuous monitoring
Kyung Cheol CHOI - for contributions to emissive, flexible, and wearable displays
Tetsuo Endoh - for contributions to nonvolatile memory and spintronic logic
Harald Gossner - for contributions to ESD design of advanced IC devices and high speed systems

Masataka Higashiwaki- for contributions to gallium oxide electronics and milimeter-wave gallium nitride transistors
Andras Kis - for contributions to the development of 2D materials and electronic devices
Guann-pyng Li - for contributions to the bipolar device, circuit and technology in silicon and compound semiconductors
Takashi Matsuoka - for contributions to laser diodes for optical communications and nitride semiconductors for light emitting devices
Thomas Mikolajick - for contributions to nonvolatile memory
Yoshiaki Nakano - for contributions to semiconductor integrated photonic devices and circuits
Kenichi Okada - for contributions to millimeter-wave communication circuits design
Boon S. Ooi - for contributions to broadband light emitters and visible light communications
Guann Pyng Li - for contirbutions to the bipolar device, circuit and technology in silicon and compound semiconductors
Munaf T Rahimo - for contributions to high-voltage insulated gate bipolar transistors for grid applications
Sei-Hyung Ryu - for contributions to silicon carbide power device technology
Abu Sebastian - for contributions to in-memory computing for scientific applications
Dmitri Strukov - for contributions to neuromorphic and alternative computing systems based on emerging memory devices
Richard Syms - for contributions to mass spectrometers based on microelectromechanical system technology
Miguel Urteaga – for contributions to terahertz heterojunction bipolar transistor integrated circuit technology
Pierre Verlinden - for leadership in high performance silicon solar cell and photovoltaics technology and commercialization
Hua Wang - for contributions to high-efficiency microwave and millimeter-wave power amplifiers
Qiangfei Xia - for contributions to resistive memory arrays and devices for in-memory computing

Plenary Papers

Technical Program Chair: Kirsten Moselund, Paul Scherrer Institute (PSI) / EPFL

9:30 AM
1-1 Redefining Innovation: A Journey forward in New Dimension Era (Invited), Siyoung Choi, President and GM Foundry Business, Device Solutions Division, Samsung Electronics

The semiconductor industry has been experiencing drastic changes of the surrounding economic and geo-political circumstances, and it has become more essential because of its permeating role in numerous other industries. In particular, the incessant foundry progress has been maintained through a series of fundamental technology breakthroughs from materials to structures, taming several complicated difficulties associated with technical and cost barriers. The track records set by foundries' technology developments are clear for all to see, and their positive impact on our lives is immeasurable.

10:20 AM
1-2 Making Memory Magic and the Economics Beyond Moore's Law (Invited), Thy Tran, Vice President of Global Frontend Procurement, Micron Technology

The global semiconductor industry, driven by compute, automotive, data storage, and wireless markets, is projected to exceed a trillion-dollar in sales revenue by 2030 (Fig. 1), [1]. The mainstream memory industry bit shipment has increased by 12x for DRAM and 48x for NAND flash in the past decade [2] and this bit growth trend needs to be sustained through continued scaling in the future to meet the projected demands of global data creation (Fig. 2). In addition, generating value from the data is driving the need for memory to be closer to the compute and increase data bandwidth, speed, and energy per bit metrics. Delivering higher bandwidth and speed at lower energy while minimizing power has become a major challenge with respect to continued scaling of memory, which also must deliver year over year cost reduction at faster cadence. In this paper, we touch on

DRAM and NAND scaling challenges and industry trends to tackle the power, performance, area, cost, and time (PPACt) requirements through design and technology co-optimization (DTCO). Such requirements are also driving memory development to explore advanced interconnect and innovative packaging solutions.

11:10 AM
1-3 Semiconductor Challenges in the 5G and 6G Technology Platforms (Invited), Bjorn Ekelund Corporate Research Director, [1]Ericsson AB, Sweden

The global semiconductor industry, driven by compute, automotive, data storage, and wireless markets, is projected to exceed a trillion-dollar in sales revenue by 2030 (Fig. 1), [1]. The mainstream memory industry bit shipment has increased by 12x for DRAM and 48x for NAND flash in the past decade [2] and this bit growth trend needs to be sustained through continued scaling in the future to meet the projected demands of global data creation (Fig. 2). In addition, generating value from the data is driving the need for memory to be closer to the compute and increase data bandwidth, speed, and energy per bit metrics. Delivering higher bandwidth and speed at lower energy while minimizing power has become a major challenge with respect to continued scaling of memory, which also must deliver year over year cost reduction at faster cadence. In this paper, we touch on DRAM and NAND scaling challenges and industry trends to tackle the power, performance, area, cost, and time (PPACt)requirements through design and technology co-optimization (DTCO). Such requirements are also driving memory development to explore advanced interconnect and innovative packaging solutions.

Technical Sessions

Session 2: Advanced Logic Technology (ALT) - Gate-All-Around and New Channel Material Devices
1:30 PM, Grand Ballroom A
Co-Chairs: Anne Vandooren, IMEC and Byounghak Hong, Samsung

This session covers recent advances in 2D transition metal dichalcogenide (TMD) and gate-all-around (GAA) devices to further extend Moore's law, consisting of six papers both from industry and academia. Two papers highlight 2D channel material devices. The first paper focuses on MoS2 single channel performance optimization and demonstrates 2 -monolayer stacked channels formation thanks to highly selective channel release. The second paper addresses manufacturability of 2D materials at 300mm wafer scale. The next three papers focus on Si nanosheet GAA transistors. The first one is an invited paper which identifies challenges to further scale GAA devices from a patterning perspective with EUV insertion. The second one demonstrates the performance benefits of a nanosheet technology optimized for a 77K operating temperature. The third paper is a systematic study of the impact of Si (001) and (110) orientation on nanosheet NFET and PFET showing an overall better performance on (001) substrate orientation. The last paper of the session presents a new fabrication process of GeOI FinFETs based on layer transfer to eliminate channel defects and maximize device performance at 10K.

1:35 PM
2-1 Monolayer-MoS_2 Stacked Nanosheet Channel with C-type Metal Contact, Yun-Yan Chung[1], Wei-Sheng Yun[1], Bo-Jhih Chou[2], Chen-Feng Hsu[1], Shao-Ming Yu[1], Goutham Arutchelvan[1], Ming-Yang Li[1], Tsung-En Lee[1], Bo-Jiun Lin[1], Chen-Yi Li[2], Aslan Wei[1], D. Mahaveer Sathaiya[1], Cheng-Ting Chung[1], San-Lin Liew[1], Vincent D.-H. Hou[1], Wen-Hao Chang[3], Bo-Heng Liu[4], Chien-Wei Chen[4], Chien-Ying Su[4], Chi-Chung Kei[4], Jin Cai[1], Chung-Cheng Wu[1], Jeff Wu[1], Tung-Ying Lee[1], Chao-Hsin Chien[2], Chao-Ching Cheng[1], Iuliana P. Radu[1]
[1]Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, [2]Institute of Electronics National Yang Ming Chiao Tung University, Hsinchu, Taiwan, [3]Department of Electrophysics National Yang Ming Chiao Tung University, Hsinchu, Taiwan, [4]Taiwan Instrument Research Institute, National Applied Research Laboratories, Hsinchu, Taiwan

First demonstrates stacked-nanosheet-devices with 1L-MoS_2 after release 2 nanosheets simultaneously. Two-stacked 1L-MoS_2 nanosheets can be released 150nm, proving excellent mechanical properties. Conformal-gate-stack-deposition on 2-stacked MoS_2-sheets is confirmed. 'C-type' wrap-around-contact is demonstrated

for contact-area-increasing. First time, gate-stack and its impact on SS, Vth and hysteresis are presented on single-GAA-NSFET with postive-Vth.

2:00 PM

2-2 Exploring manufacturability of novel 2D channel materials: 300 mm wafer-scale 2D NMOS & PMOS using MoS_2, WS_2, & WSe_2

Chelsey Dorow[1], Tom Schram[2], Quentin Smets[2], Kevin O'Brien[1], Kirby Maxey[1], Chia-Ching Lin[3], Luca Panarella[2,4], Ben Kaczer[2], Nazmul Arefin[1], Anandi Roy[3], Rob Jordan[5], Adedapo Oni[5], Ashish Penumatcha[1], Carl Naylor[1], Mahmut Kavrik[1], Daire Cott[2], Benjamin Groven[2], Valeri Afanasiev[2,4], Pierre Morin[2], Inge Asselberghs[2], Cesar Lockhart de la Rosa[2], Gouri Sankar Kar[2], Matthew Metz[3], Uygar Avci[3,]
Intel, [2]IMEC, [3]Components Research, Intel Corporation, [4]KU Leuven, [5]Intel Corporation

We scale up to 300 mm both NMOS and PMOS 2D transistors using today's leading TMD candidates: MoS_2, WS_2, and WSe_2. MoS_2 outperforms WS_2 for NMOS while WSe_2 multi-layers show high PMOS on-currents reaching 200 μA/μm. Larger TMD grain sizes show up to 10× higher on-currents and steeper SS.

2:25 PM

2-3 Scaling opportunities for Gate-All-Around and beyond: A patterning perspective (Invited)

Indira Seshadri[1], Eric Miller[1], Jennifer Church[1], Jingyun Zhang[1], Andrew Greene[1], Julien FROUGIER[1], Tao Li[1], Yasiel Cabrera[1], Martin Burkhardt[1], Spyridon Skordas[1], Luciana Meli[1], Nelson Felix[1]
[1]IBM

Here, we review how EUV (extreme ultraviolet) lithography especially in the front end of line simplifies gate all around fabrication. We discuss avenues to the further scaling of GAA - High Numerical Aperture (NA=0.55) EUV and chiplet integration.

2:50 PM

2-4 High Performance Nanosheet Technology Optimized for 77 K

Ruqiang Bao[1], Liqiao Qin[2], Julien FROUGIER[2], Sung Dae Suk[2], Mohamed Rabie[2], Utkarsh Bajpai[2], Anthony Chou[2], Bettina Nechay[3], Mohamed Mohamed[4], Ruturaj Pujari[2], Terence Weir[4], Karen Harmon[4], Aditya Varma[4], Wayne Armstrong-Moore[3], Alberto Cestero[2], Susan Emans[2], Prateek Hundekar[2], R Joshi[2], Juntao Li[2], Xuan Liu[2], Steve Lucarini[2], Carl Radens[2], Shahab Siddiqui[2], Henry Trombley[2], Andres Bryant[2], Mohammad Hasanuzzaman[2], Amlan Majumdar[2], Min Gyu Sung[2], Jingyun Zhang[2], Effendi Leobandung[2,]
[1]IBM Research, [2]IBM, [3]Northrop Grumman, [4]MIT Lincoln Laboratory

We demonstrated high performance Nanosheet technology at 77 K with dual work function metals (WFMs) and dual dipoles at 77 K. Nanosheet with low V_{DD} (0.3 - 0.4 V) at 77 K provides comparable performance to that at 300K with V_{DD}=0.75V, but at much lower power.

3:40 PM

2-5 Evaluation of (110) versus (001) Channel Orientation for Improved nFET/pFET Device Performance Trade-Off in Gate-All-Around Nanosheet Technology

Shogo Mochizuki[1], Nicolas Loubet[1], Pial Mirdha[1], Curtis Durfee[1], Huimei Zhou[1], Gen Tsusui[1], Julien FROUGIER[2], Reinaldo Vega[2], Liqiao Qin[2], Nelson Felix[2], Dechao Guo[1], Huiming Bu[1,]
IBM Research, [2]IBM

Stacked gate-all-around nanosheet (NS) pFET and nFET transistors have been fabricated on (110) and (001) substrates to determine the device performance dependence on Si channel orientation for short and long-channel NS devices.

4:05 PM

2-6 First Demonstration of Defect Elimination for Cryogenic Ge FinFET CMOS Inverter Showing Steep Subthreshold Slope by Using Ge-on-Insulator Structure

Xin-Ren Yu[1], Chin-Cheng Hsieh[2], Min-Hui Chuang[3], Min-Yu Chiu[4], Tsung-Chieh Sun[2], Wei-Zhe Geng[1], Wen-Hsin Chang[5], Yu-Jen Shih[1], Wen-Hsiang Lu[1], Wei-Chieh Chang[1], Yu-Chuan Lin[1], Yu-Chia Pai[1], Chia-Yen Lai[6], Chiung-Yi Yang[1], Yun Dei[7], Nien-Chih Lin[8], Hao-Yu Lu[9], Ming-Han Chuang[1], William Cheng-Yu Ma[10], Chien-Ting Wu[8], Kuo-Hsing Kao[1], Darsen D. Lu[1], Yao-Jen Lee[8,11], Guang-Li Luo[8], Meng-Hsueh Chiang[1], Tatsuro Maeda[5], Wen-Fa Wu[8], Yi-Ming Li[3], Tuo-Hung Hou[8], Yeong-Her Wang[1,]
[1]Dept. of Electrical Engineering, National Cheng Kung University, [2]Academy of Innovative Semiconductor and Sustainable Manufacturing, National Cheng Kung University, [3]Institute of Communications Engineering, National Yang Ming Chiao Tung University, [4]Dept. of Electrical Engineering, National Sun Yat-Sen University, [5]National Institute of Advanced Industrial Science and Technology, [6]Institute of Artificial Intelligence Innovation, National Yang Ming Chiao Tung University, [7]Institute of Biomedical Engineering, National Yang Ming Chiao Tung University, [8]Taiwan Semiconductor Research Institute, [9]Intelligent Computing Industrial Doctorate Program, Miin Wu School of Computing, National Cheng Kung University, [10]Dept. of Electrical Engineering, Natl. Sun Yat-Sen University, [11]Institute of Pioneer Semiconductor Innovation, National Yang Ming Chiao Tung University

This work presents experimental electrical characteristics and circuit prediction at cryogenic temperatures for three different kinds of germanium (Ge)-based FETs with advanced Fin/GAA structures. Among them, the layer-transferred GeOI FinFET significantly improves its I-V characteristic during cryogenic measurements. The developed GeOI fabrication method provides an effective way to eliminate the defects originating from misfit dislocations at the Ge/Si substrate during epitaxial growth, which would be treated as the key to device performance enhancement under 10 K. According to the measured IV at 10 K and circuit prediction, GeOI FinFETs with high Ge crystallinity are strong candidates for High-Performance-Computing applications.

Session 3: Modeling and Simulation (MS) - 2-D materials for advanced logic and quantum applications
1:30 PM, Grand Ballroom B
Co-Chairs: Devin Verreck, IMEC and Francois Triozon, CEA-Leti

The session includes 4 papers on the modeling of 2-D materials for advanced logic and quantum computing applications. The first 2 papers discuss conventional logic scaling, while the last 2 assess the potential of 2-D materials for quantum computing and spin logic. The first paper, by Gilardi and Zeevi of Stanford University, is a DTCO optimization of a dielectric barrier layer to improve EDP. The second paper, by Knobloch of TU Wien (invited), presents an overview of TCAD and compact model approaches to benchmark performance and reliability. The third paper, by Agashiwala of University of California Santa Barbara, evaluates 2-D materials for cryo-CMOS interface electronics in quantum computing, highlighting the advantages to conventional semiconductors. The fourth paper, by Zhang of University of California Santa Barbara, assesses 2-D materials for spin logic and interconnects, showing significant improvements in EDP and spin diffusion lengths.

1:35 PM
3-1 Barrier Booster for Remote Extension Doping and its DTCO in 1D & 2D FETs
Carlo Gilardi[1], Gilad Zeevi[1], Suhyeong Choi[1], Sheng-Kai Su[2], Terry Hung[2], Shengman Li[1], Nate Safron[3], Qing Lin[1], Tathagata Srimani[1], Matthias Passlack[3], Gregory Pitner[3], Edward Chen[2], Iuliana Radu[2], H.-S. Philip Wong[1], Subhasish Mitra[1,]
[1]Stanford University, [2]Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, [3]Taiwan Semiconductor Manufacturing Company Limited, San Jose, CA, USA

We present *dielectric barrier booster* for remote extension doping in low-dimensional materials. Leveraging extensive DTCO, barrier booster enables 1.5× energy-delay product (EDP) benefits vs. no-barrier case. We derive insights and doping guidelines for Carbon Nanotube and MoS_2 FETs and we project 1.9× and 4.6× EDP benefits respectively vs. extension-undoped FETs.

2:00 PM
3-2 Modeling the Performance and Reliability of Two-Dimensional Semiconductor Transistors (Invited)

Theresia Knobloch[1], Dominic Waldhoer[1], Mohammad Davoudi[1], Alexander Karl[1], Pedram Khakbaz[1], Manuel Matzinger[1], Yichi Zhang[2], Kirby K Smithe[3], Aftab Nazir[4], Chris Liu[4], Yury Yuryevich Illarionov[5], Eric Pop[3], Hailin Peng[2], Ben Kaczer[6], Tibor Grasser[1,]
[1]TU Wien, [2]Peking University, [3]Stanford University, [4]Huawei Technologies R&D, [5]SUSTech University, [6]IMEC

2D materials offer high mobilities and drive currents in atomically thin layers, allowing for excellent gate control. To enable the transition from prototypes to integrated circuits at an industrial scale, physical predictive modeling tools are required. We show how TCAD and compact models can be used to describe the performance.

2:25 PM
3-3 Advancing High-performance Large-Scale Quantum Computing with Cryogenic 2D-CMOS
Kunjesh Agashiwala[1], Arnab Pal[1], Hang Cui[1], Tanmay Chavan[1], Wei Cao[1], Kaustav Banerjee[1,]
[1]UC Santa Barbara
This paper provides the first comprehensive insight into 2D-semiconductors (2DS) as a cryogenic-CMOS-interface-electronics platform to enable large-scale quantum-computing. Using rigorous ab-initio and transport simulations, we demonstrate that 2DS-FETs operate at ultralow supply-voltages with minimal noise introduced to qubits along with significantly reduced device-to-device mismatch, leading to unmatchable energy-efficiency and performance.

2:50 PM
3-4 A Materials-Device Co-Design Framework for Realizing Ultra Energy-Efficient All-2D-Spin-Logic Circuits with 2D-Materials
Shuo Zhang[1], Arnab Pal[2], Wenyan Yin[1], Wei Cao[2], Kaustav Banerjee[2,]
[1]Zhejiang University, [2]University of California, Santa Barbara

This work introduces a materials-device co-design framework for optimizing spin-transistors and -interconnects employing 2D-materials. It is shown that optimized 2D-spin-transistors outperform MOSFETs by yielding more than two-orders of magnitude improvement in energy-efficiency, while Gr spin interconnects can provide diffusion lengths exceeding 25 µm, thereby paving the way for all 2D-spin-logic.

Session 4: Reliability Of Systems and Devices (RSD) - Protection from ESD, Thermal Runaway and Corrosion
1:30 PM, Continental 1-3
Co-Chairs: Bonnie Weir, Broadcom and Susanna Reggiani, Università di Bologna

The session starts with the analysis of various ESD-protection devices dealing with the most innovative technologies and covers prevention of thermal runaway and corrosion. The first paper from K.U. Leuven, by W-C. Chen, addresses the protection of extremely thin wafers with double-sided connectivity. The next paper, from the University of Illinois, by S. Huang, proposes a novel silicon-controlled rectifier in a finFET technology. The third paper, from NYCU-Taiwan, by Tz-Wun Wang, proposes an ESD-protection methodology for monolithic GaN-on-Silicon. Stephen Poon (TSMC) follows with an invited talk, which gives a general view of ESD reliability in advanced nodes. The fifth talk from Stanford University, by K. Woo, moves on to present innovations in diamond-based cooling to prevent thermal runaway. The final talk from Purdue University, by M. Asaduz Zaman Mamun, presents a holistic approach to prevent wirebond corrosion failure.

1:35 PM
4-1 ESD Challenges in 300nm Si Substrate of DTCO/STCO Scaling Options
Wen-Chieh Chen[1], Shih-Hung Chen[2], Anabela Veloso[2], Kateryna Serbulova[3], Geert Hellings[4], Guido Groeseneken[1,]
[1]KULeuven/imec, [2]Imec, [3]KULeuven/Imec, [4]imec
In DTCO/STCO era, sub-µm Si substrate is essential for vertical connections. This work first- time evaluates the ESD performance of various ESD devices with 300nm wafer thickness and nTSV. The thermal dissipation of these ESD devices with BS contact/ metals were studied for a possible solution to the thermal issue.

2:00 PM

4-2 Poly-Bounded Silicon-Controlled-Rectifier for ESD Protection in FinFET Technology

Shudong Huang[1], Srivatsan Parthasarathy[2], Yuanzhong Zhou[2], Jean-Jacques Hajjar[2], Elyse Rosenbaum[1],
[1]University of Illinois at Urbana-Champaign, [2]Analog Devices Inc.

A low-capacitance, low trigger voltage, and fast turn-on silicon-controlled rectifier (SCR) is developed for electrostatic discharge (ESD) protection in a FinFET technology. A deep-Nwell biasing technique is introduced. The proposed SCR device can sink more than 10-A of VFTLP current at 5V and with less than 80-fF of capacitive loading.

2:25 PM

4-3 ESD HBM 3kV Discharge for Monolithic GaN-on-Si HEMTs Integrated Chips

Tz-Wun Wang[1], Chang-Lin Go[1], Sheng-Hsi Hung[1], Chi-Yu Chen[1], Po-Jui Chiu[1], Ke-Horng Chen[1], Kuo-Lin Zheng[1,2], Ying-Hsi Lin[3], Tsung-Yen Tsai[3], Shian-Ru Lin[3],
[1]NYCU, [2]Chip-GaN Power Semiconductor, [3]Realtek Semiconductor

This paper proposes ESD protection in GaN-on-silicon processes. Due to well-designed ESD circuits and tunable geometry of GaN devices, the disadvantage of large I_Q in conventional ESD schemes can be reduced to 8.11μA, a 222x improvement, by an area-efficient implementation, and discharge 3kV and 100V HBM and MM tests, respectively.

3:15 PM

4-4 ESD Reliability in Advanced Nodes (Invited)

Steven Szehang Poon[1], Ming-Hong Kao[1], Wei-Chao Chang[1], T.F. Huang[1],
[1]TSMC

Standard ESD protection structures continue to perform well in advanced technologies. However, Power, Performance, and Area (PPA) considerations have increased the importance of accurately deploying a sufficient but not excessive amount of ESD protection. This invited paper will describe how device and product ESD qualification efforts support these critical changes.

3:40 PM

4-5 Interlayer Engineering to Achieve <1 m^2K/GW Thermal Boundary Resistances to Diamond for Effective Device Cooling

Kelly Woo[1], Mohamadali Malakoutian[1], Youhwan Jo[2], Xiang Zheng[3], Thomas Pfeifer[4], Ramandeep Mandia[5], Taesoon Hwang[2], Henry Aller[6], Daniel Field[3], Patrick Hopkins[4], Samuel Graham[6], Martin Kuball[3], Kyeongjae Cho[2], Srabanti Chowdhury[1]
[1]Stanford University, [2]UT Dallas, [3]University of Bristol, [4]University of Virginia, [5]Arizona State University, [6]University of Maryland, College Park

Highly localized electric fields and resulting high temperatures can degrade semiconductor devices, leading to premature failure. Diamond with its high thermal conductivity is an effective device/chip level heat-spreader when integrated at the channel/junction. However, a bottleneck lies in the thermal boundary resistance between the hotspot and the heat spreader. Atomistic thermal transport modeling was used to show the reduction of TBR below the diffuse-mismatch theory predictions is possible with a SiC interlayer. Experimentally, the interlayer crystallinity and thickness were engineered to produce TBRs of 3.1±0.7 and 1.89±0.18m^2K/GW. This can lead to W-band power to >30 W/mm in GaN HEMTs.

4:05 PM

4-6 A Holistic Approach to Predict Wirebond Corrosion Failure in Extreme Operating Environments

Md Asaduz Zaman Mamun[1], Amar Mavinkurve[2], René Rongen[2], Michiel van Soestbergen[2], Muhammad A. Alam[1]
[1]Purdue University, [2]NXP Semiconductors

In this study, we: (i) investigate in-situ ion migration behavior in the EMC (under various use conditions) using measured leakage current across the metal-EMC-metal capacitive structure, (ii) determine migrated/ localized ions near the bond pad using 3D numerical simulation, (iii) encapsulate the insights from the simulations and the assumption of a first-order redox reaction into a failure distribution model, and (iv) provide physics-based reasoning for the power-law observed in the empirical accelerated failure model. The proposed model is validated by IC failure data from multiple companies, i.e., Cisco, Motorola, NXP, and Huawei.

Session 5: Neuromorphic Computing (NC) - Neuromorphic Hardware
1:30 PM, Continental 4
Co-Chairs: Sanghyeon Kim, KAIST and Eric Vogel, Georgia Tech

This session covers bioinspired neuromorphic technologies featuring novel device demonstrations. The first paper describes a dendrite-like device that discriminates spatiotemporal patterns of pulses for parallel processing. The second paper experimentally demonstrated ReRAM devices enabling scalable online e-Prop learning algorithms. The third is an invited paper which describes the fundamental relationship between the switching dynamics of redox-based memristive devices and their analog programming capability for neuromorphic applications. The fourth paper demonstrates that back-end-of-the-line oscillatory neurons based on InGaAs biristors and coupled via capacitive synapses are suitable for solving complex pattern recognition tasks. The final paper demonstrates a multifunction three-dimensional vertical random-access memory array where different layers exhibit nonvolatile properties and volatile characteristics, respectively, can be used to implement multimodal neuromorphic computing tasks such as video recognition.

1:35 PM
5-1 Multi-gate FeFET Discriminates Spatiotemporal Pulse Sequences for Dendrocentric Learning
Hugo J.-Y. Chen[1], Matthew Beauchamp[1], Kasidit Toprasertpong[1], Fei Huang[1], Louis Le Coeur[1], Thorgund Nemec[2], H.-S. Philip Wong[1], Kwabena Boahen[1]
[1]Stanford University, [2]GlobalFoundries

This paper presents a dendrite-like device that discriminates spatiotemporal patterns of pulses for parallel processing in 3D neuromorphic architectures. The device utilizes the ferroelectric layer in a segmented multi-gate FeFET design to detect a consecutive sequence of input pulses. Experimental results demonstrate successful emulation of highly selective sequence discrimination in dendrites of neurons in the cortex and highlight up to 100× signal-margin (output current differences). This nanodendrite design offers a neuromorphic solution to thermally scalable parallel processing in 3D systems.
2:00 PM
5-2 ReRAM-Based NeoHebbian Synapses for Faster Training-Time-to-Accuracy Neuromorphic Hardware
Tinish Bhattacharya[1], Sai Sukruth Bezugam[1], Shubham pande[1,2], Ewelina Wlazlak[1], Dmitri Strukov[1],
[1]UC Santa Barbara, [2]IIT Madras

For the first time, NeoHebbian artificial synapses based on ReRAM devices have been proposed and demonstrated, enabling scalable online e-Prop learning. These synapses, with two state variables, use either a pair of ReRAM devices in different configurations or a heater-assisted design for weight updates. Benchmarks show these synapses significantly reduce training time and energy in temporal data modeling applications.

2:25 PM
5-3 Engineering the kinetics of redox-based memristive devices for neuromorphic computing (Invited)
Regina Dittmann[1], Alexandros Sarantopoulos[2], Christopher Bengel[3], Alexander Gutsche[2], Felix Cüppers[2], Susanne Hoffmann-Eifert[2], Stephan Menzel[2],
[1]Forschungszentrum Jülich, [2]Forschungszentrum Jülich GmbH, [3]RWTH Aachen University

For neuromorphic computing applications, analog programming characteristics with linear updates are highly desirable. Here, we discuss the relation between the switching dynamics of redox-based memristive devices and their analog programming capability. We identify three groups of devices based on the valence change mechanism with characteristic properties. Experimental results and theoretical considerations suggest that analog switching can be achieved if a thermal runaway is avoided. Moreover, we argue that internal series resistances play a crucial role in controlling the runaway and determining the accessible resistance window.

2:50 PM

5-4 BEOL-compatible 4F² Single Crystalline Semiconductor Oscillator for Low-power and Large-scale Oscillatory Neural Network Hardware

Joon Pyo Kim[1], Hyun Wook Kim[2], Jaeyong Jeong[1], Juhyuk Park[1], Seong Kwang Kim[1], Jongmin Kim[3], Jiyong Woo[2], Sanghyeon Kim[1]
[1]KAIST, [2]KNU, [3]KANC

Oscillatory neural network (ONN) is suitable for solving complex patterns. In this work, we demonstrated the feasible ONN hardware based on an InGaAs biristor, a single-crystal semiconductor exhibiting high reliability, uniformity, and repeatability. We expect that the advantages of the InGaAs biristor-based oscillator in terms of its cell size (4F2), low-temperature fabrication (< 100 ℃), and high reliability will contribute to future advancements in 3D stackable ONN hardware systems.

3:15 PM

5-5 High Area Efficiency (6 TOPS/mm²) Multimodal Neuromorphic Computing System Implemented by 3D Multifunctional RRAM Array

Wenxuan Sun[1,2], Yi Li[1], Xiaoxin Xu[1]
[1]State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, [2]University of Chinese Academy of Sciences, Beijing, China

For the first time, we demonstrated a multifunction three-dimensional (3D) vertical random-access memory (RRAM) array (MF-3DRRAM) where different layers exhibit nonvolatile properties and volatile characteristics respectively to implement multimodal neuromorphic computing. The RRAM cells in the 1st layer (WL: TiN) and the 2nd layer (WL: Ru) have different dynamic characteristics, which are used to construct multi-scale reservoirs (M-RC). The RRAM in 3rd layer (WL: W) exhibits analog switching behavior, applying for convolutional neural network (CNN) and full connection (FC) layer. A multimodal neuromorphic computing system with the network of M-RC+CNN is implemented by the MF-3DRRAM. The multifunction of the fabricated MF-3DRRAM chip is validated through the multimodal video recognition task, exhibiting high accuracy (98%), high area efficiency (6 TOPS/mm²) and low energy consumption (1.4pJ/operation). This proposed MF-3DRRAM is of great significance for miniaturized, low-power hardware implementations for edge computing.

Session 6: Memory Technology (MT) - DRAM

1:30 PM, Continental 5
Co-Chairs: DerChang Kau, Intel Corp and Haitao Liu, Micron

This Session includes 7 papers in the advances of DRAM technology. We will start with 3 approaches to deliver 4F^2 cell. Samsung Electronics Co. (SEC) will introduce tri-gate and gate all around access device while CXMT will exhibit the recent advances in vertical channel access devices. SEC will also demonstrate vertical IGZO channel device for DRAM technology beyond 10nm. To mitigate the constraint wordline resistance in DRAM, SK Hynix Inc.'s work-function engineering of metal gate is explored to improve DRAM performance at scaling. Last but not least, there are 3 exciting papers on capacitor-less DRAM. Macronix International Co. and SEC use Thyristor based DRAM cell enabling 3D DRAM integration beyond 10nm. Institute of Microelectronics of Chinese Academy of Sciences uses 2T0C IGZO channel demonstrates 4bits/cell with retention >1000s.

1:35 PM

6-1 Self-Aligned in 2Pitch Cell Array Transistor (S2CAT) for 4F2 Based DRAM Generation Extension

Seokhan Park[1]
[1]Samsung

This paper presents a novel $4F^2$ cell transistor for future DRAM. The self-aligned in 2-pitch cell array transistor (S2CAT) in this work uses a back-gate (BG) shared by two neighboring cells to control threshold voltage (V_T) and the spacers of BG was employed as masks for the Si vertical channels.

2:00 PM
6-2 High-Performance Gate-all-around Junctionless Vertical-Channel Transistors with the Ultra-low Sub-threshold Swing for Next-generation $4F^2$ DRAM
Abraham Yoo[1], Jiang Yi[1], Yunsong Qiu[1], Yuhong Zheng[1], Chen Yang[1], Daohuan Feng[1], Yucheng Liao[1], Xiangbo Kong[1], Jianfeng Xiao[1], Dongsheng Xie[1], Jinying Liu[1], Jian Chu[1], Di Ma[1], Minrui Hu[1], Wenli Zhao[1], Guangsu Shao[1], Chao Lin[1], Kai Shao[1], Yan Wang[1], Handong Xu[1], Zelun Li[1], Kuoming Huang[1], Xingkun Xue[1], Tingting Gu[1], Kang You[1], Xiang Liu[1], Jong Sung Jeon[1], Shufang Si[1], Yanzhe Tang[1], Mingde Liu[1], Yadong Guo[1], Jintao Chen[1], Mingtang Zhang[1], Xinwen Jin[1], GJ Yang[1], DH Han[1], Ted Park[2], Deyuan Xiao[1], Chao Zhao[2], Kanyu Cao[1]
[1]CXMT, [2]BJSAMT

In this paper, we have successfully fabricated the junction-less GAA VCT combined with a hexagonal capacitor to realize a compact $4F^2$ DRAM architecture. It shows the breakthroughs of $I_{on}/I_{off}>10^9$ and SS=62.5 mV/dec. We also elaborated on various key process issues and device parameters and how they impact on performance.

2:25 PM
6-3 Highly Manufacturable, Cost-Effective, and Monolithically Stackable $4F^2$ Single-Gated IGZO Vertical Channel Transistor (VCT) for sub-10nm DRAM
Daewon Ha[1], Wonsok Lee[1], Min Hee Cho[1], Masayuki Terai[1], Sung-Won Yoo[1], Hwan Kim[1], Yongjin Lee[1], Sanghoon Uhm[1], Mintae Ryu[1], Changhyuck Sung[1], Younggeun Song[1], Kiseok Lee[1], Sang Wuk Park[1], Kong-Soo Lee[1], YongSuk Tak[1], Eunsuk Hwang[1], Jiwon Chae[1], Changik Im[1], Seong Jae Byeon[1], Minji Hong[1], Kihyung Sim[1], Woo Je Jung[1], Huije Ryu[1], Moonju Hong[1], Sungjoon Park[1], Jaeho Pak[1], YOONHWAN CHOI[1], Seungwon Lee[1], Gunjoo Woo[1], Juho Lee[1], Dae Sin Kim[1], Bong Jin Kuh[1], Yu Gyun Shin[1], Jaihyuk Song[1]
[1]Samsung Electronics

For the first time, we demonstrated experimentally $4F^2$ single-gated IGZO-VCT, monolithically stacked on top of core/peripheral transistors without wafer bonding process for sub-10nm DRAM.

2:50 PM
6-4 A Workfunction Engineered Middle-Silicon-TiN Gate (MSTG) Cell Transistor in 16Gbit DRAM for High Scalability and Long Data Retention
Seong-Wan Ryu[1], Kyung Kyu Min[1], Sunghwan Hwang[1], Hyunmin Seung[1], Sungsoo Yoon[1], Yoonjae Nam[1], Jungmin Moon[1], Yaeji Kim[1], Euntae Kim[1], Jongkook Park[1], Kyoungchul Jang[1], Sinwoo Kang[1], Taekyun Kim[1], Seonsoon Kim[1], Ilsup Jin[1], Seonyong Cha[1]
[1]SK hynix Inc.

To mitigate constraint of the increased gate resistance for dual-workfunction-gate cell transistors as a DRAM standard platform, a middle-silicon-TiN gate, which replaces the n+-polysilicon with ultra-thin TiN/silicon interlayer/TiN was demonstrated in fully integrated 1x-nm 16Gb and provides superior retention time without sacrificing gate resistance compared to the single workfunction gate.

3:40 PM
6-5 A Highly Pitch-Scalable Capacitor-less 3D DRAM Using Cross-bar Selection with Gate-Controlled Thyristor (GCT) Featuring High Endurance and Free Read-Disturb
Wei-Chen Chen[1], Hang-Ting Lue[1], Ming-Hung Wu[1], Yu-Tang Lin[1], Keh-Chung Wang[1], Chih-Yuan Lu[1]
[1]Macronix

We enhanced the 3D DRAM GCT by incorporating cross-bar array selection, achieving self-rectifying IBL-VBL curves, low leakage, and enabling vertical-BL 3D DRAM for improved sensing and pitch scaling. It holds promise for high-layer stacking and DRAM-based computing in memory.

4:05 PM

6-6 3-STAR : A Super-steep switching, Stackable, and Strongly Reliable Transistor Array RAM for Sub-10nm DRAM and beyond

Kyunghwan Lee[1], Sungwon Yoo[1], Jaeho Hong[1], Hyun-cheol Kim[1], YongSeok Kim[1], Ilgweon Kim[1], Daewon Ha[1], Yu-Gyun Shin[1], Jaihyuk Song[1]
[1]Samsung Electronics

We proposed and reviewed a novel capacitor-less DRAM named 3-STAR. It has VCT structure and is stackable, so it is very advantageous for footprint. The memory characteristics are dramatically improved thanks to trap layer insertion. It is a highly promising candidate device for the next-generation DRAM device.

4:30 PM

6-7 First Demonstration of True 4-bit Memory with Record High Multibit Retention >10^3s and Read Window >10^5 by Hydrogen Self-Adaptive-Doping for IGZO DRAM Arrays

Gangping Yan[1,2,3], Yanna Luo[1], Jianjian Wang[1], Zhiyu Song[1], Chuqiao Niu[1], Shangbo Yang[1], Guoliang Tian[1], Jiaxin Yao[1], Xueli Ma[2], Qingzhu Zhang[1], Jinjuan Xiang[2], Na Zhou[1], Guilei Wang[2], Gaobo Xu[1], Zhenhua Wu[1,4], Jinshun Bi[3], Chao Zhao[2], Jun Luo[1], Huaxiang Yin[1]
[1]Institute of Microelectronics of Chinese Academy of Sciences, [2]Beijing Superstring Academy of Memory Technology, Beijing 100176, China, [3]University of Chinese Academy of Sciences, [4]School of Integrated Circuits, University of Chinese Academy of Sciences

For the first time, we demonstrate a true 4-bit memory with large operation margin, and record-long multibit retention with largest window in IGZO-based 2T0C DRAM. It is enabled by a low-cost oxygen-compensated hydrogen self-adaptive-doping (OHAD) method. Due to controllable compensation for defects and enhanced source/drain doping, the best-in-class devices exhibit the V_{TH} modulated to +0.23V and I_{on} boosted to 35μA/μm, with smallest variation of $\sigma(V_{TH})$=25mV and $\sigma/\mu(I_{on})$=4%. It yields a record-high memory window >10^5 and retention of 10^4s with largest margin, capable of first 16-level separated states for realizing true 4-bit 2T0C cells with record-long 1000-s retention in multibit operation.

Session 7: Focus Session 4: Neuromorphic Computing for Smart Sensors - SMB/NC/EDT - Focus Session - Neuromorphic Computing for Smart Sensors

1:30 PM, Continental 6
Co-Chairs: Hidehiro Fujiwara, TSMC and Xiaoting Jia, Virginia Tech

This focus session includes 6 invited papers that describe recent advances in neuromorphic computing and smart sensors. The first paper from Università di Pisa and Quantavis s.r.l. discusses the fabrication of analog neuromorphic circuits based on a standard silicon CMOS process, heterostructures of two-dimensional materials (2DMs), and a hybrid technology. They show floating-gate FETs – both in silicon and 2DMs – as promising analog non-volatile memories (NVMs) enabling good analog computing precision. The second paper from Samsung Advanced Institute of Technology describes a novel analog in-sensor computing architecture, enhancing the existing fully parallel analog processing system by incorporating analog circuits to store layer outputs. The third paper from Sony presents image recognition processing and its algorithm compression technique incorporating computing capabilities for efficient processing in CMOS image sensors for edge devices. The fourth paper from Brown University, Northeastern University, Raytheon BBN, and Boston University reviews state-of-the-art examples of capacitive imaging arrays and presents new demonstrations of all-electrical imaging of growing bacterial cultures. The next paper, from Carnegie Mellon University, presents a novel capacitance biosensor for characterizing DNA origami. Their biosensor was fabricated in a 0.18um CMOS process and they also demonstrate a self-referencing data acquisition scheme to reduce the variance in DNA origami measurements. The last paper from University of Maryland proposes two sensors, ISFET and capacitive sensor arrays for measuring pH and real time monitoring of cell growth.

1:35 PM
7-1 The case for hybrid analog neuromorphic chips based on silicon and 2D materials (Invited)
Giuseppe Iannaccone[1]
[1]University of Pisa

We discuss the challenges and the opportunities of the hybrid integration of 2D materials into a CMOS technology platform with the aim of equipping devices at the edge of the cloud with cognitive capabilities, through innovations in architectures, circuits and technology.

2:00 PM
7-2 Case study of tactile sensors: system level approach to analog in sensor computing (Invited)
Min Young Mun[1], Sei Joon Kim[1], Seok Ju Yun[1], Sang Joon Kim[1]
[1]Samsung Electronics

We propose a novel analog in-sensor computing architecture, enhancing the existing fully parallel analog processing system by incorporating analog circuits to store the outputs of layers. Through simulations using tactile sensors, we demonstrate a 65% reduction in area and superior power efficiency, twice as efficient as the previous work.

2:25 PM
7-3 Intelligent Vision Sensor and Edge Computing Envisage the Future (Invited)
Ryoji Eki[1], Ryohei Kawasaki[1], Eita Yanagisawa[1]
[1]Sony Semiconductor Solutions

We present a method of edge computing and its algorithm compression technique, which incorporates computing capabilities for efficient processing in CMOS image sensors. Furthermore, we demonstrate the evolution of image recognition processing resulting from the advancement of devices on showcasing practical examples utilizing event-based vision sensors.

3:15 PM
7-4 Live-Cell Imaging with Integrated Capacitive Sensor Arrays (Invited)
Jacob K Rosenstein[1], Joseph Larkin[2], Yongchao Yin[3], Slava Epstein[3], Meni Wanunu[3], Aaron Adler[4]
[1]Brown University, [2]Boston University, [3]Northeastern University, [4]Raytheon Technologies

Integrated capacitive imaging arrays offer intriguing possibilities for cell culture monitoring, offering low cost, portability, single-cell resolution, a wide field of view, and co-integration with multiple electrochemical sensing and stimulation modes. Here we review the state of the art, and present new demonstrations of all-electrical imaging of growing bacterial cultures.

3:40 PM
7-5 Towards CMOS Capacitance Sensors for DNA Origami Characterization (Invited)
Marc Dandin[1], Md Sakibur Rahman Sajal[1], Kai-Chun Lin[1], Yann Gilpin[1], Vismaya Walawalkar[1], Fahimeh Dehghandehnavi[1], Rebecca Taylor[1,]
[1]Carnegie Mellon University

This work features a novel capacitance biosensor for characterizing DNA origami.

4:05 PM
7-6 Scalable biosensors using standard CMOS process (Invited)
Utku Noyan[1], Sheung Lu[1], Jennifer Blain Christen[2], Pamela Abshire[1], Sahil Shah[1,]
[1]University of Maryland, College Park, [2]Arizona State University

In this study, we introduce two distinct biosensors fabricated using the standard CMOS process: an Ion-Sensitive Field-Effect Transistors (ISFETs) and a Capacitive sensor array, both developed in a 0.5µm process. Expanding on its practical application, we employ integrated sensors to perform real-time monitoring of cell culture.

Session 8: Optoelectronics, Displays, and Imaging Systems (ODI) - Advanced Photonics for Image Sensors and High-Speed Communications
1:30 PM, Continental 7-9
Co-Chairs: Andreas Mai, IHP microelectronics and Douglas Paul, University of Glasgow

This session chairs 6 papers describing advanced photonics for image sensors applications and high-speed communications. The first three papers deal with device and integration concepts for different sub-diffraction color filters targeting imaging key performance indicators. The first paper by IMEC demonstrates color splitting to match the human eye color sensitivity space with a Vora value >95% using a novel sub-micrometer integration approach. The second paper by VisEra Technologies presents the use of nano-light pillars to improve the quantum efficiency and the signal-to-noise ratio (SNR) under low light conditions of color filters on CMOS imaging arrays. Next, Samsung demonstrates a metasurface nano-prism structure for wide field of view lenses to demonstrate 25% higher sensitivity and 1.2 dB increased SNR compared to conventional micro-lenses. The final three papers demonstrate devices and technologies for high speed communication systems. The 4th paper from the National University of Singapore presents the integration of ferroelectric material into a LiNbO3 on insulator photonic platform demonstrating non-volatile memory and high efficiency modulators with an efficiency of 66 pm/V. The 5th paper from IHP demonstrates the first germanium electro-optical modulator operating at 100 GHz in a SiGe BiCMOS photonics technology. The last paper from Intel (invited) demonstrates the first 256 Gbps WDM transceiver with eight 200 GHz-spaced wavelengths simultaneously modulated at 32 Gbps and a bit-error-rate less than 1e-12.

1:35 PM
8-1 Wafer-level-integrated vertical-waveguide sub-diffraction-limited color splitters
Shuo Kang[1], Meryem Benelajla[2,3], Rossa Mac Ciamain[1], Farhan Ali[1,4], Athina Papadopoulou[1,4], Oksana Shramkova[1], Liesbeth Witters[1], Joeri De Vos[1], Pawel E. Malinowski[1], Paul Heremans[1,4], Nicolas Le Thomas[2,3], Bruno Figeys[1], Robert Gehlhaar[1], Jan Genoe[1,4]
[1]imec, [2]Ghent University, [3]Center for Nano- and Biophotonics, [4]KULeuven

We demonstrate a new technology for splitting colors with sub-micron resolution using standard backend processing. The color splitting is tunable via the geometry and can be designed to correspond to the color sensitivity of the human eye. The technology results in: higher signal-to-noise ratio, better color quality and enhanced resolution

2:00 PM
8-2 CMOS image sensor with nano light pillars for optical performance enhancement
Chun-Yuan Wang[1,1], Guang-Yu Huang[1], Chung-Hsuan Yu[1], Hao-Wei Liu[1], Yu-Shen Lu[1], Wei-Lung Tsai[1], An-Li Kuo[1], Shin-Hong Kuo[1], Han-Son Chen[1], Huang-Jen Chen[1], Po-Hsiang Wang[1], Ching-Chiang Wu[1], Ken Wu[1], Hung-Jen Tsai[1]
[1]VisEra Technology Co., Ltd

We have demonstrated a CMOS image sensor (CIS) with nano-light pillars (NLPs), which are metasurface-like structures, on a 0.8 μm-pixel sensor to enhance quantum efficiency. By employing a unique arrangement of NLPs, the light energy can be selectively directed to specific color pixels based on the design wavelength. The NLPs improve the quantum efficiency (QE) by 40% and 16% for blue and green, respectively, compared to micro-lens (ML) type of sensors. The luminance signal-to-noise ratio (SNR) improves by +1.16 dB under low-light conditions (20 lux) without compromising color fidelity.

2:25 PM

8-3 Optical design of dispersive metasurface nano-prism structure for high sensitivity CMOS image sensor

Chulsoo Choi[1], Jonghoon Park[1], Yunki Lee[1], Bumsuk Kim[1], Junghoon Kim[1], Sunwook Kim[1], Junghyun Kim[1], Sookyoung Roh[2], Sungmo Ahn[2], Sangeun Mun[2], Beomsuk Lee[3], Seungjoo Nah[4], Howoo Park[4], Hyunchul Kim[3], Changrok Moon[3], Seokho Yun[2], Jungchak Ahn[1], Joonseo Yim[1]
[1]SAMSUNG System LSI Division, [2]Samsung Advanced Institute of Technology, [3]Samsung Semiconductor R&D Center, [4]Samsung Foundry Division

In this paper, a meta-photonic structure called nano-prism (NP) is designed and experimentally applied on 0.64μm pixel image sensor having 50Mp with 5mm 4mm size as a replacement of conventional μ-lens. In this paper, NP design and improved pixel characteristics in the oblique light condition are described. Also, NP pattern adjustable spectral response is verified. Furthermore, innovatively improved quantum efficiency (QE) improvement that resulted in 25% of sensitivity and 1.2dB of signal to noise ratio (SNR) improvement, and other important sensor characteristics such as auto-focus and resolution are also demonstrated in this paper.

3:15 PM

8-4 First Demonstration of HZO-LNOI Integrated Ferroelectric Electro-Optic Modulator and Memory to Enable Reconfigurable Photonic Systems

Zefeng Xu[1], Chun-Kuei Chen[1], Hong-Lin Lin[1], Yuan Gao[1], Wei Ke[2], Baochang Xu[1], Pavel Dmitriev[1], Carlan Arbiz[3], Evgeny Zamburg[1], Steven Touzard[1], Xinlun Cai[2], James Lee[3], Suresh Venkatesan[3], Aaron Danner[1], Aaron Voon-Yew Thean[1]
[1]National University of Singapore, [2]Sun Yat-sen University, [3]POET Technologies

We have successfully demonstrated, for the first time, an innovative back-end-of-line compatible electro-optic modulator and memory (EOMM) based on Lithium Niobate on Insulator micro-ring resonator integrated with Ferroelectric Hafnium Zirconate non-volatile analog memory. We have also tested the integration of the EOMM with POET technologies' 400G Tx/Rx optical interposer chip.

3:40 PM

8-5 Photonic BiCMOS Technology with 80 GHz Ge Photo Detectors and 100 GHz Ge Electro-Absorption Modulators

Daniel Steckler[1], Stefan Lischke[1], Anna Peczek[1], Aleksandra Kroh[1], Lars Zimmermann[1,2]
[1]IHP-Leibniz Institut für innovative Mikroelektronik, [2]Technische Universität Berlin

We demonstrate a Photonic BiCMOS technology featuring waveguide-coupled germanium electro-absorption modulators and photo detectors with respective 3-dB bandwidths of 100 GHz and 80 GHz, monolithically integrated with high-performance SiGe-heterojunction bipolar transistors and 0.25 μm CMOS.

4:05 PM

8-6 A silicon photonic 8&[lambda] x 32Gbps/&[lambda] WDM transceiver with integrated laser array and SOA for optical I/O (Invited)

Haisheng Rong[1], Duanni Huang[1], Zhe Xuan[1], Ranjeet Kumar[1], Cooper Levy[1], Guan-Lin Su[1], Chaoxuan Ma[1], Xinru Wu[1], Songtao Liu[1], Sharma Jahnavi[1], Jinyong Kim[1], Tolga Acikalin[1], Ganesh Balamurugan[1], James Jaussi[1]
[1]Intel

We demonstrate a 256Gbps WDM transceiver with eight 200GHz spaced wavelengths simultaneously modulated at 32Gbps and <1e-12 BER. The system includes a silicon photonic PIC with integrated lasers, ring modulators, SOAs, and a co-designed EIC.

Session 9: Power, Microwave/Mm-Wave and Analog Devices/Systems (PMA) - GaN Power Devices Integration

1:30 PM, Imperial A
Co-Chairs: Rongming Chu, Penn State and Hongping Zhao, The Ohio State University

This session includes 7 papers that describe the advancements in GaN power electronic devices and integration technology. The first paper, by Dr. Tim McDonald from Infineon, outlines the role that latest power semiconductor technologies and circuits play in achieving a sustainable energy future. The second paper demonstrates a novel GaN/SiC hybrid field-effect transistor that can harness the complementary merits of GaN and SiC. In the third paper, a bipolar p-FET device with enhanced conduction capability is presented. The fourth paper demonstrates larger gate swing and enhance threshold voltage stability of GaN HEMTs using a metal/insulator/p-GaN structure. The next two papers report monolithically integrated GaN half bridges, on sapphire and Si substrates, respectively. The last paper, from Intel, showcases industry's first CMOS "DrGaN" technology fabricated in a 300 mm GaN-on-Si process containing enhancement-mode GaN MOSHEMT with 3D monolithic integration of Si PMOS.

1:35 PM

9-1 Power Conversion Semiconductor and Circuit Trends and Challenges for a Sustainable Energy Future

Timothy Kevin McDonald[1], Timothy Kevin McDonald[1]
[1]Infineon Technologies

To meet total global energy requirements with zero or reduced carbon emissions will necessarily result in a dramatic increase in the use of high efficiency power conversion technology. This work will outline the role that latest power semiconductor technologies and circuits play in achieving such a sustainable energy future. Several relevant example applications will be considered based on devices and related circuit topologies. Barriers to the rate of adoption is briefly considered. Looking forward, future advances in device technology are discussed with up-to-date information.

2:00 PM

9-2 HyFET—A GaN/SiC Hybrid Field-Effect Transistor

Sirui Feng[1,2], Zheyang Zheng[1], Yuru Wang[1], Gang Lyu[1], Kai Liu[3], Yan Cheng[1], Junting Chen[1,4], Tao Chen[1], Li Zhang[1], Wenjie Song[1], Hang Liao[1], Yat Hon Ng[1], Mengyuan Hua[4], Kai Cheng[3], Jin Wei[5], Kevin J. Chen[1]
[1]The Hong Kong University of Science and Technology, [2]Hong Kong University of Science and Technology, [3]Enkris Semiconductor. Inc., [4]Southern University of Science and Technology, [5]School of Integrated Circuits, Peking University, Beijing, China

This work presents a GaN/SiC hybrid field-effect transistor (HyFET)—a novel power electron device that can harness the complementary merits of GaN and SiC and circumvent their notorious drawbacks. Our experimental demonstration unveils a new power device platform enabling the utmost integration of these two prevailing wide-bandgap semiconductors.

2:25 PM

9-3 Bipolar p-FET with Enhanced Conduction Capability on E-mode GaN-on-Si HEMT Platform

Mengyuan Hua[1], Jinjin Tang[1], Zuoheng Jiang[1], Chengcai Wang[1], Junting Chen[1,1], Haohao Chen[1], Yihan Zhang[2], Zheyang Zheng[2], Xinyu Wang[1], Jun Ma[1], Junlei Zhao[1], Jianxun Liu[3], Qian Sun[3]
[1]Southern University of Science and Technology, [2]The Hong Kong University of Science and Technology, [3]Suzhou Institute of Nano-Tech and Nano-Bionics

A bipolar p-FET (BiPFET) structure is proposed to enhance the conduction capability of GaN-based p-channel transistors that is limited by the intrinsically low hole mobility. A n-/p-/n-GaN (NPN) bipolar stack is depolyed at the drain side of a conventional p-FET, amplifying the conduction current with electrons serving as the majority carriers, which possess much higher mobility than holes. By matching the NPN stack with p-FET, the drain current density increases by 17 times compared to the conventional p-FET, exceeding 100 mA/mm. Meanwhile, device control logic, high I_{ON}/I_{OFF} ratio and low gate leakage current of the p-FET are also well preserved.

2:50 PM

9-4 Simultaneously Achieving Large Gate Swing and Enhanced Threshold Voltage Stability in Metal/Insulator/p-GaN Gate HEMT

Junjie Yang[1], Jin Wei[1], Maojun Wang[1], Teng Li[1], Jingjing Yu[1], Xuelin Yang[2], Jinyan Wang[1], Yilong Hao[1], Bo Shen[2]
[1]School of Integrated Circuits, Peking University, Beijing, China, [2]School of Physics, Peking University, Beijing, China

A metal/insulator/p-GaN gate HEMT (MIP-HEMT) with built-in p-GaN potential stabilizer (PPS) is demonstrated to simultaneously achieve a large gate swing and an enhanced V_{TH} stability. The MIP-gate structure enlarges the gate swing to 19.5 V. The PPS eliminates the floating p-GaN effects, resulting in a superior VTH stability.

3:40 PM

9-5 1200V E-mode GaN Monolithic Integration Platform on Sapphire with Ultra-thin Buffer Technology

Sheng Li[1], Yanfeng Ma[1], Weihao Lu[1], Mingfei Li[1], Lixi Wang[1], Zikang Zhang[1], Tinggang Zhu[2], Yiheng Li[2], Jiaxing Wei[1], Long Zhang[1], Siyang Liu[1], Weifeng Sun[1]
[1]Southeast University, [2]CorEnergy Semiconductor Co., LTD

1200V E-mode GaN monolithic halfbridge integration platform on Sapphire with ultra-thin buffer is firstly proposed. The breakdown voltage of p-GaN HEMT reaches over 2000V (0.1μA/mm@175℃). The crosstalk and substrate-biasing effects of halfbridge are suppressed (even @175℃). The monolithic halfbridge circuit works under 800V-switching conditions at 175℃ successfully.

4:05 PM

9-6 650-V GaN-on-Si Power Integration Platform Using Virtual-Body p-GaN Gate HEMT to Screen Substrate-Induced Crosstalk

Junjie Yang[1], Jin Wei[1], Maojun Wang[1], Muqin Nuo[1], Han Yang[2], Teng Li[1], Jingjing Yu[1], Xuelin Yang[2], Yilong Hao[1], Jinyan Wang[1], Bo Shen[2]
[1]School of Integrated Circuits, Peking University, Beijing, China, [2]School of Physics, Peking University, Beijing, China

A 650-V GaN power integration platform is demonstrated on a standard low-resistivity bulk Si substrate using virtualbody p-GaN Gate HEMTs (VB-HEMTs). The holes injected from the p-GaN gate accumulate and spread along the virtual body, providing an effective screening against substructure-induced crosstalk up to 400 V.

4:30 PM

9-7 DrGaN: an Integrated CMOS Driver-GaN Power Switch Technology on 300mm GaN-on-Si with E-mode GaN MOSHEMT and 3D Monolithic Si PMOS

Han Wui Then[1], Marko Radosavljevic[1], Samuel Bader[1], Ahmad Zubair[1], Heli Vora[1], Nityan Nair[1], Pratik Koirala[1], Michael Beumer[1], Paul Nordeen[1], Andrey Vyatskikh[1], Thomas Hoff[1], Jason Peck[1], Thoe Michaelos[1], Emmannuel Khora[1], Rob Jordan[1], Rambert Nahm[1], Curtis Hoffman[1], Noel Franco[1], Adedapo Oni[1], Samuel Beach[1], Divya Garg[1], Dimitri Frolov[1], Alvaro Latorre-rey[1], Alex Mitaenko[1], Jag Rangaswamy[1], Soumen Sarkar[1], Shahriar Ahmed[1], Vincent Rayappa[1], Hsiang Chiu[1], Alex Hubert[1], Sean Brophy[1], Nazmul Arefin[1], Nachiket Desai[1], Harish Krishnamurthy[1], Jingshu Yu[1], Krishnan Ravichandran[1], Paul Fischer[1]
[1]Intel Corporation

We demonstrate industry's first CMOS "DrGaN" fabricated in 300mm GaN-on-Silicon process combining GaN-MOSHEMT with 3D-monolithic Si-PMOS by layer-transfer. The 180nm DrGaN achieves R_{DSON}=0.8 mohm-mm^2 and leakage<0.1mA. A gate-last process is demonstrated where high-temperature steps are completed before ALD-deposition of gate-dielectric for GaN-MOSHEMT. FOM=1/($R_{ON}Q_{GG}$)=0.59 (mohm-nC)$^{-1}$ is achieved for L_G 30nm GaN-MOSHEMT.

Session 10: Emerging Device and Compute Technology (EDT) - Low Dimensional Material Device Technology

1:30 PM, Imperial B
Co-Chairs: Han Wang, University of Southern California and Jaehyun Park, Samsung

This session includes 6 papers that focus on low dimensional material-based device technology. The first four papers address key technology challenges in 2D material-based logic transistors. The first paper by TSMC presents the latest update on the status of 2D material integration modules and the device performance for advanced logic transistor applications. The second paper, by Purdue University, reports record performance WSe2 p-FET device fabricated through a hybrid charge transfer and molecular doping method. The third paper, through a collaboration between TU Wien and Intel, describes a reliability study of double-gated wafer-scale MoS2 transistors. The fourth paper, by Intel, reports TMD CMOS GAA architecture for logic applications. The last two papers of the session describe the progress in carbon nanotube-based logic transistor technology. The fifth paper, by TSMC, discussed low n-type contact resistance to carbon nanotube transistors via doping in the dielectric. The last paper, led by Stanford University, reports carbon nanotube transistors with high on-state current achieved through a self-alinged doping process.

1:35 PM
10-1 Status and Performance of Integration Modules Toward Scaled CMOS with Transition Metal Dichalcogenide Channel
Ang-Sheng Chou[1], Ching-Hao Hsu[1,2], Yu-Tung Lin[1,2], Goutham Arutchelvan[1], Edward Chen[1], Terry Y.T. Hung[1], Chen-Feng Hsu[1], Sui-An Chou[1], Tsung-En Lee[1], Oreste Madia[3], Gerben Doornbos[3], Yuan-Chun Su[1,4], Amin Azizi[5], D. Mahaveer Sathaiya[6], Jin Cai[1], Jer-Fu Wang[1], Yun-Yan Chung[1], Wen-Chia Wu[1,7], Katie Neilson[5], Wei-Sheng Yun[1], Yu-Wei Hsu[2], Ming-Chun Hsu[2], Fa-Rong Hou[2], Yun-Yang Shen[4], Chao-Hsin Chien[7], Chung-Cheng Wu[6], Jeff Wu[6], H.-S. Philip Wong[1], Wen-Hao Chang[4], Mark van Dal[3], Chao-Ching Cheng[1], Chih-I Wu[2], Iuliana P. Radu[1]
[1]Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, [2]National Taiwan University, [3]Pathfinding, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, [4]Department of Electrophysics National Yang Ming Chiao Tung University, Hsinchu, Taiwan, [5]Taiwan Semiconductor Manufacturing Company Limited, San Jose, CA, USA, [6]TCAD, Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, [7]Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

This work demonstrates comparable n-type and p-type high-performance on 2D transistors. Translation to 300 mm wafer processing is tested by die-by-die transfer of the 2D material. The 300 mm fabrication preserves relatively high mobility. And demonstrate scaling of nMOS contact-length to 12 nm and top gate-length to 10 nm.

2:00 PM
10-2 Wafer-scale CVD Monolayer WSe_2 p-FETs with Record-high 727 μA/μm I_{ON} and 490 μS/μm g_{max} via Hybrid Charge Transfer and Molecular Doping
Hao-Yu Lan[1], Rahul Tripathi[1], Xiangkai Liu[1], Joerg Appenzeller[1], Zhihong Chen[1]
[1]Birck Nanotechnology Center, Purdue University

This study introduces a novel hybrid p-doping strategy, integrating WOx charge transfer and NO molecular doping with wafer-scale CVD 1L-WSe2, enabling a record-high *I*ON of 727 μA/μm and a record-high *g*m of 490 μS/μm, while maintaining an excellent on-off current ratio of ~ 9 orders of magnitude.

2:25 PM
10-3 Reliability Assessment of Double-Gated Wafer-Scale MoS_2 Field Effect Transistors through Hysteresis and Bias Temperature Instability Analyses
Alexandros Provias[1], Theresia Knobloch[1], Ande Kitamura[2], Kevin P O'Brien[2], Chelsey Dorow[2], Dominic Waldhoer[1], Bernhard Stampfer[1], Ashish Penumatcha[2], Sudarat Lee[2], Rahul Ramamurthy[2], Scott Clendenning[2], Michael Waltl[1], Uygar Avci[2], Tibor Grasser[1]
[1]TU Wien, [2]Components Research, Intel Corp

2D field-effect transistors (FETs) based on transition metal dichalcogenides (TMDs) are a potential replacement for silicon transistors at sub-12 nm channel lengths. We demonstrate initial reliability and performance for double-gated NMOS FETs based on MoS_2 as channel with a HfO_2 back gate and a Al_2O_3/HfO_2 top gate stack fabricated in an industry lab. We present a comprehensive analysis of hysteresis curves obtained at varying conditions as well as bias temperature instability measurements. Our analysis reveals excellent stability in terms of hysteresis and good BTI behavior relative to published 2D FETs, even though it is still higher than commercial $Si/SiO_2/HfO_2$ stacks.

3:15 PM

10-4 High Mobility TMD NMOS and PMOS Transistors and GAA Architecture for Ultimate CMOS Scaling

Ashish Penumatcha[1], Kevin P O'Brien[1], Kirby Maxey[1], Wouter Mortelmans[1], Rachel Steinhardt[1], Sourav Dutta[2], Chelsey Dorow[1], Carl Naylor[1], Ande Kitamura[1], Ting Zhong[1], Pratyush Buragohain[3], Carl Rogan[1], Chia-Ching Lin[3], Mahmut Kavrik[1], Jennifer Lux[1], Adedapo Oni[4], Andrey Vyatskikh[1], Sudarat Lee[1], Nazmul Arefin[5], Paul Fischer[1], Marko Radosavljevic[3], Scott Clenndenning[1], Mathew Metz[1], Uygar Avci[6]
[1]Components Research, Intel Corp, [2]Components Research, Intel, [3]Components Research, Intel Corporation, [4]Technology Development, Intel Corp, [5]Global Sourcing for Equipment and Materials, Intel Corp, [6]Intel

We present high-mobility MOCVD PMOS WSe_2 with hole mobility of 50 cm^2/Vs and ON-current of 247 μA/μm. We also show CVD MoS_2 with electron mobility ~45 cm^2/Vs, along with the first reported TMD PMOS Gate-All - Around transistor with SSlin~107mV/dec. TMD IDVG data is compared to silicon to identify improvements needed.

3:40 PM

10-5 Low N-Type Contact Resistance to Carbon Nanotubes in Highly Scaled Contacts through Dielectric Doping

Nathaniel S. Safron[1], Hsin-Yuan Chiu[2,3], Tzu-Ang Chao[2,4], Sheng-Kai Su[2], Matthias Passlack[1], Kuang-Hsiang Chiu[5], Chien-Wei Chen[6], Chi-Chung Kei[6], Chen-Han Chou[5], Tsung-En Lee[2], Jer-Fu Wang[2], Chih-Sheng Chang[2], San-Lin Liew[2], Vincent D.-H. Hou[2], Han Wang[1], Wen-Hao Chang[7], H.-S. Philip Wong[2], Gregory Pitner[1], Chao-Hsin Chien[5], Iuliana P. Radu[2]
[1]Taiwan Semiconductor Manufacturing Company, San Jose, CA, USA, [2]Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, [3]Institute of Electronics, National Yang Ming Chiao Tung University, [4]Department of Electrophysics, National Yang Ming Chiao Tung University, [5]Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, [6]Taiwan Instrument Research Institute, National Applied Research Laboratories, Hsinchu, Taiwan, [7]Department of Electrophysics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

Carbon nanotube transistors with low n-type contact resistance (Rc) of 9.7 kΩ/CNT with short contact length (Lc) of 20nm is achieved by utilizing AlN solid-state n-doping. We systematically explore doping control, Rc trends scaling down to 20nm Lc, and symmetric Rc n- and p-FET towards the IRDS 2034 roadmap target.

4:05 PM

10-6 High-performance and low parasitic capacitance CNT MOSFET: 1.2 mA/μm at V_{DS} of 0.75 V by self-aligned doping in sub-20 nm spacer

Shengman Li[1], Tzu-Ang Chao[2], Carlo Gilardi[1], Nathaniel Safron[3], Sheng-Kai Su[2], Gilad Zeevi[1], Andrew Denis Bechdolt[1], Matthias Passlack[2], Aaryan Oberoi[3], Qing Lin[1], Zichen Zhang[4], Kesong Wang[4], Harshil Kashyap[4], San-Lin Liew[2], Vincent D.-H. Hou[2], Prabhakar Bandaru[4], Andrew Kummel[4], Iuliana Radu[2], Gregory Pitner[3], H.-S. Philip Wong[1,2], Subhasish Mitra[1]
[1]Stanford University, [2]Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, [3]Taiwan Semiconductor Manufacturing Company Limited, San Jose, CA, USA, [4]University of California, San Diego, CA, USA

For the first time we report degenerate and self-aligned doping in the sub-20nm spacer region on a high-density CNT channel to achieve high-performance CNT p-MOSFET with I_D = 1.2 mA/μm at V_{DS} = -0.75 V, CGP = 160 nm, and L_G = 50 nm.

Tuesday, Dec. 12
Session 11: Memory Technology (MT) - Ferroelectric-based Memory Technology
9:00 AM, Grand Ballroom A
Co-Chairs: Yu-Ming Lin, TSMC and Wenke Weinreich, FhG IPMS

This session includes 7 papers covering recent developments for various ferroelectric-based memory technologies. The first two papers address key issues of 1T FeFET to improve endurance and retention characteristics by 2D channel material and noble metal electrodes, respectively. The next three papers cover fundamental studies on ferroelectric capacitor for cross-point array applications. Key challenges like disturb and endurance are addressed by various technology and operation strategies. Also, frequency-dependent characterization techniques are used to understand fundamental interfacial properties in ferroelectric materials. The session is finalized by one paper presenting FTJ device integrated with OTS selector achieving high retention and another one on integrated 1T1C 3D FeRAM in Mb array with high reliability.

9:05 AM
11-1 High-Endurance MoS_2 FeFET with Operating Voltage Less Than 1V for eNVM in Scaled CMOS Technologies
Tsung-En Lee[1], Hung-Li Chiang[1], Chih-Yu Chang[1], Yuan-Chun Su[1,2], Shu-Jui Chang[1], Jui-Jen Wu[1], Bo-Jiun Lin[3], Jer-Fu Wang[1], Shu-Chih Haw[4], Shang-Jui Chiu[4], He-Liang Ching[4], Yan-Gu Lin[4], Wei-Sheng Yun[1], Chen-Feng Hsu[1], Hengyuan Lee[5], Tung-Ying Lee[5], Matthias Passlack[6], Chao-Ching Cheng[1], Chih-Sheng Chang[6], H.-S. Philip Wong[1], Wen-Hao Chang[2], Meng-Fan Marvin Chang[7], Yu-Ming Lin[5], Iuliana Radu[1]
[1]Taiwan Semiconductor Manufacturing Company Limited, Hsinchu, Taiwan, [2]Department of Electrophysics National Yang Ming Chiao Tung University, Hsinchu, Taiwan, [3]Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, [4]National Synchrotron Radiation Research Center, [5]Taiwan Semiconductor Manufacturing Company, [6]Taiwan Semiconductor Manufacturing Company Limited, [7]tsmc

For the first time, we demonstrate a TMD FeFET with ultra-high endurance and retention time exceeding 10 years. The devices are fabricated through HZO on AlO_x/ MoS_2 with T < 250°C. By using a 2.5nm HZO layer and a 1L-MoS_2, a record-low VWRITE < 1V is reported.

9:30 AM
11-2 First Demonstration of Annealing-Free Top Gate La:HZO-IGZO FeFET with Record Memory Window and Endurance,
Min Zeng[1,2], Qianlan Hu[1], Qijun Li[2], Honggang Liu[2], Shiwei Yan[2], Chengru Gu[2], Wenjie Zhao[2], Ru Huang[1], Yanqing Wu[1]
[1]Peking University, [2]Huazhong University of Science and Technology

In this work, we demonstrate annealing-free La:HZO capacitors with record $2P_r$ of 30 μC/cm^2 and also La:HZO-IGZO based top-gate FeFET with record memory window (MW) of 3.3 V, record-high endurance of 10^{10} while maintaining large MW of 1.9 V and 10^8 with MW of 3.1 V for the first time.

9:55 AM
11-3 First Demonstration of Hafnia-based Selector-Free FeRAM with High Disturb Immunity through Design Technology Co-Optimization
Fu Zhiyuan[1], Shengjie Cao[1], Hao Zheng[1], Jin Luo[1], Qianqian Huang[1,2,3], Ru Huang[1,2,3]
[1]Peking University, [2]Beijing Advanced Innovation Center for Integrated Circuits, [3]Beijing Superstring Academy of Memory Technology

In this work, a high-disturb-immunity FE-HZO capacitor is demonstrated based on comprehensive investigation based on newly proposed pulse-disturb analysis method. Further 3D-stackable 1-kbit cross-point array for

selector-free FeRAM based on the optimized FE-HZO devices is experimentally demonstrated with read/write, showing significantly disturb-immunity through DTCO and pulse-recovery pulsing protocol.

10:20 AM

11-4 Pulse-Based Capacitive Memory Window with High Non-Destructive Read Endurance in Fully BEOL Compatible Ferroelectric Capacitors

Shankha Mukherjee[1,2], Jasper Bizindavyi[1], Yuan-Chun Luo[3], Sergiu Clima[1], James Read[3], Mihaela I Popovici[1], Yang Xiang[1], Nina Bazzazian[1], Attilio Belmonte[1], Romain Delhougne[1], Gouri Sankar Kar[1], Francky Catthoor[1,2], Valeri V Afanas'ev[1,2], Shimeng Yu[3], Jan Van Houdt[1,2]
[1]IMEC, [2]KU Leuven, [3]Georgia Institute of Technology

We report on the pulse-based non-destructive read of a record high capacitive memory window in a BEOL compatible HZO-based ferroelectric capacitor. Contrary to conventional reading schemes, we show that the non-destructive read operation enables a full decoupling between the read- and write-endurance and we demonstrate a read-endurance beyond 1e11 cycles.

11:10 AM

11-5 AC Impedance Characteristics of Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$: from 1 kHz to 10 GHz

Taekyong Kim[1], Elham Rafie Borujeny[1,2], Ignacio Sardinero-Meirás[3], Jesús Grajal[3], Kenneth Cadien[2], Dimitri Antoniadis[1], Jesús del Alamo[1]
[1]Massachusetts Institute of Technology, [2]University of Alberta, [3]Universidad Politécnica de Madrid

We conducted extensive AC impedance characterization of W/FE-HZO/W structures from 1 kHz to 10 GHz. We have found that butterfly-shaped C-V persists up to the highest frequencies but its frequency dependence is extinguished around 1 GHz. We also find that AC conductance(σac) increases with frequency. The frequency dispersion of capacitance is consistent with electron trapping at border traps near the W/HZO interface. The butterfly-shaped C-V in GHz range is postulated to arise from electron depletion and accumulation at the W/HZO interface. The frequency dependence of σac is consistent with the universal dielectric response theory through the correlated barrier hoping model.

11:35 AM

11-6 Superior retention (>1 year, 85ºC) and memory window (~1.8 V) using ultra-thin HZO FTJ with OTS selector for X-point memory applications

Laeyong Jung[1], Jangseop Lee[1], Seungyeol Oh[1], Hyunsang Hwang[1]
[1]POSTECH

We present excellent nonvolatile memory characteristics using ultra-thin $Hf_xZr_{1-x}O_2$ (HZO) ferroelectric tunneling junction (FTJ) device and SiTeAsGe (STAG) ovonic threshold switching (OTS) selector. To increase on-current of FTJ, thickness-scaling is required. To avoid leakage-current of unselected device, we adopted OTS selector. By matching the off-state current of both FTJ and OTS devices by controlling film thickness and area, we can maximize the threshold voltage (V_{th}) window up to 1.8V and achieve retention over 1year at 85℃. Moreover, excellent reliability characteristics (>10^8 endurance) and fast switching speed (<10ns) were confirmed. These comprehensive findings highlight the strong potential for X-point memory application.

12:00 PM

11-7 A highly reliable 1.8 V 1 Mb $Hf_{0.5}Zr_{0.5}O_2$-based 1T1C FeRAM Array with 3-D Capacitors

Jun Okuno[1], Takafumi Kunihiro[1], Tsubasa Yonai[1], Ryo Ono[1], Yusuke Shuto[1], Ruben Alcala[2], Maximilian Lederer[3], Konrad Seidel[3], Thomas Mikolajick[2,4], Uwe Schroeder[2], Masanori Tsukamoto[1], Taku Umebayashi[1]
[1]Sony Semiconductor Solutions Corporation, [2]NaMLab gGmbH, [3]Fraunhofer IPMS - Center Nanoelectronics Technologies, [4]TU Dresden

This study proposes a novel 1 Mb one-transistor one-capacitor ferroelectric random access memory array based on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ with 3D cylindrical capacitors. We obtain a perfect functionality with a

sufficient memory window at a small projected cylinder area at an operating voltage of 1.8 V with high reliability.

Session 12: Neuromorphic Computing (NC) - Bayesian networks and physical unclonable functions
9:00 AM, Continental 1-3
Co-Chairs: Daniele Ielmini, Politecnico Milano and Po-Hao Tseng, Macronix

This session presents novel computing techniques leveraging the stochastic switching and fluctuations of memory devices to enable Bayesian networks and physical unclonable functions. The first paper 'Hardware Demonstration of Feedforward Stochastic Neural Networks with Fast MTJ-based p-bits' by N. Singh et al. presents a Bayesian feedforward network based on a stochastic magnetic tunnel junction (sMTJ). The second paper 'Memcapacitor Crossbar Array with Charge Trapping Layer for Physical Unclonable Function in NAND Flash Architecture' by M. S. Song et al. introduces a new physical unclonable function (PUF) based on the stochastic native states of a memcapacitive flash memory for security applications. The invited paper 'Bayesian In-Memory Computing with Resistive Memories' by C. Turck et al. provides an overview of recently proposed Bayesian approaches using resistive memories to evaluate decision uncertainty in safety critical applications. The fourth paper 'First Demonstration of a Bayesian Machine based on Unified Memory and Random Source Achieved by 16-layer Stacking 3D Fe-Diode with High Noise Density and High Area Efficiency' by T. Gong et al., demonstrates a 16-layer stacking 3D ferroelectric diode array for noise-driven Bayesian computing machine. Finally, the fifth paper 'Bayesian Neural Network Implemented by Dynamically Programmable Noise in Vanadium Oxide' by S. Oh et al., presents a novel approach toward Bayesian neural networks using the programmable noise in VO2-based devices.

9:05 AM
12-1 Hardware Demonstration of Feedforward Stochastic Neural Networks with Fast MTJ-based p-bits
Nihal Sanjay Singh[1], Shaila Niazi[1], Shuvro Chowdhury[1], Kemal Selcuk[1], Haruna Kaneko[2,3], Keito Kobayashi[2,3], Shun Kanai[2,3], Hideo Ohno[2], Shunsuke Fukami[2,3], Kerem Camsari[1]
[1]Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA, USA, [2]Research Institute of Electrical Communication, Tohoku University, Sendai, Japan, [3]Graduate School of Engineering, Tohoku University, Sendai, Japan

We experimentally demonstrated probabilistic inference in feedforward stochastic neural networks by parallelized and carefully ordered updates in a hybrid MTJ+FPGA computer. We also demonstrated the fastest p-bits (1 microseconds) in hardware using in-plane MTJs. Scaled up versions of our computer hold significant potential for energy-efficient inference for deep learning models.

9:30 AM
12-2 Memcapacitor Crossbar Array with Charge Trapping Layer for Physical Unclonable Function in NAND Flash Architecture
Min Suk Song[1], Suhyeon Ahn[1], Hwiho Hwang[1], Hyungjin Kim[1]
[1]Inha University

We propose memcapacitor crossbar array consisting of MOS capacitors with trapping layer for physical unclonable function in NAND flash architecture. Charging-based vector-matrix multiplication is demonstrated, and PUF operations are verified using erase-state variations. Also, we investigate the utilization of memcapacitor array within 3D NAND flash architecture in two operation modes.

9:55 AM
12-3 Bayesian In-Memory Computing with Resistive Memories (Invited)
Damien Querlioz[1], Clément Turck[1], Djohan Bonnet[2], Kamel-Eddine Harabi[1], Thomas Dalgaty[3], Théo Ballet[1], Tifenn Hirtzlin[2], Adrien Pontlevy[1], Adrien Renaudineau[1], Eduardo Esmanhotto[2], Pierre Bessière[4], Jacques Droulez[5], Raphaël Laurent[5], Marc Bocquet[6], Jean-Michel Portal[6], Elisa Vianello[2]

[1]Univ. Paris-Saclay, CNRS, [2]CEA-Leti, [3]CEA-List, [4]Sorbonne Univ., CNRS, [5]Hawai.tech, [6]Aix-Marseille Univ., CNRS

This paper explores approaches using resistive memory for Bayesian near-memory and in-memory computing, leveraging their inherent randomness: Bayesian Machines for efficient near-memory computing, Bayesian Neural Networks exploiting randomness of synapses, and Bayesian Learning utilizing Metropolis-Hastings MCMC technique, achieving competitive accuracy with conventional software methods and with evaluation of decision uncertainty.

10:20 AM

12-4 First Demonstration of a Bayesian Machine based on Unified Memory and Random Source Achieved by 16-layer Stacking 3D Fe-Diode with High Noise Density and High Area Efficiency

Tiancheng Gong[1], Qiqiao Wu[2,3], Yuanquan Huang[1], Haijun Jiang[3], Jianguo Yang[1,3], Qing Luo[1], Steve Chung[4], Ming Liu[1,2]

[1]Institute of Microelectronics of Chinese Academy of Sciences, [2]Fudan University, [3]Zhangjiang Lab, [4]National Yang Ming Chiao Tung University

In this work, a Bayesian machine based on unified memory and random source using 16-layer stacking 3D Fe-diode is experimentally demonstrated for the first time.

10:45 AM

12-5 Bayesian Neural Network Implemented by Dynamically Programmable Noise in Vanadium Oxide

Sangheon Oh[1], T. Patrick Xiao[2], Christopher Bennett[2], Alex J. Weiss[1], Sean R. Bishop[2], Patrick Sean Finnegan[2], Elliot James Fuller[1], Sapan Agarwal[2], A. Alec Talin[3]

[1]Sandia National Labs, Livermore, CA, USA, [2]Sandia National Labs, Albuquerque, NM, USA, [3]Sandia National Labs

For the first time, the dynamically programmable noise on a vanadium oxide (VO2) device is extensively studied and exploited for implementing a Bayesian neural network (BNN). We demonstrate programming of noise in a VO2 device with either resistance programming or temperature control. The VO2 device achieved a 6.4 dynamic ratio on noise. We show that this ratio is sufficient to achieve ideal numerical levels of uncertainty quantification on CIFAR-100, achieving an expected calibration error of 3.7% (ECE measures the consistency between the network's accuracy and uncertainty)

Session 13: Advanced Logic Technology (ALT) - Interconnect and Sequential 3D Stacking

9:00 AM, Continental 4

Co-Chairs: Robert Clark, TEL and Kazuyuki Tomida, Rapidus

This session includes six papers that describe recent advances in the area of interconnect and 3D stacking. The first paper by TSMC describes intercalated graphene as a conductor candidate for future interconnects. The next paper from imec demonstrates a two-metal level Ru semi-damascene interconnect with high aspect ratio at metal pitches from 18-26 nm. The third paper from AMAT describes a low resistance middle of line using PVD W liner, CVD W gapfill and W CMP. The fourth paper is given by UCLA CHIPS. The authors show fine-pitch Cu-Cu die-to-wafer bonding as a highly effective method for integrating GaN-on-Si as well as the dielet-side PDN as a low-cost and straightforward architecture for power delivery. The fifth paper by KAIST describes interlayer thickness dependence of electrical and heat dissipation characteristics in 3D sequential CFETs with Ge p-FETs on Si n-FETs. The last presentation from imec shows the challenges and solutions of Cu/SiCN Wafer-to-Wafer hybrid bonding scaling down to 400nm pitch.

9:05 AM

13-1 Intercalated Graphene as Next Generation Back-end-of-Line Conductors

Shin-Yi Yang[1], Shu-Wei Li[1], Yu-Chen Chan[1], Chuang-Han Hsu[2], Kun-Yen Liao[1], Chien-Hsin Ho[1], Cian-Yu Chen[1], Hsin-Ping Chen[1], Ming-Han Lee[1], Blanka Magyari-Kope[2], Walker Yun[3], TL Lee[3], Iuliana Radu[3], J.Z. Huang[4], Chih-I Wu[4], Winston Shue[1], Min Cao[1]

[1]Interconnect Pathfinding Division, Taiwan Semiconductor Manufacturing Company Limited, [2]TCAD, Taiwan

Semiconductor Manufacturing Company Limited, [3]Corporate Research, Taiwan Semiconductor Manufacturing Company Limited, [4]National Taiwan University

We propose a symbiotic graphene intercalation and edge-contact architecture for interconnect application. Results show: 1) film resistivity lower than Cu below 150 Å; 2) four-orders reduction on specific contact resistivity. A simulation workflow is proposed which points out n-type metals as potentially candidates to further improve intercalated graphene's electrical properties.

9:30 AM

13-2 Two-metal-level semi-damascene interconnect at metal pitch 18 nm and aspect-ratio 6 routed using fully self-aligned via

Anshul Gupta[1], Giulio Marti[1], Gilles Delie[1], Souvik Kundu[1], Stefan Decoster[1], Olalla Varela Pedreira[1], Bart Kenens[1], Anita Farokhnejad[1], Yannick Hermans[1], Bart de Wachter[1], Anton Gavrilov[1], Alicja Lesniewska[1], Yusuke Oniki[1], Antone Pacco[1], Gayle Murdoch[1], Seongho Park[1], Zsolt Tokei[1]
[1]imec

High-aspect-ratio(HAR~6-8) Ru lines(M2), at CD7-10nm,metal-pitch18-26 nm, in two-metal-level semi-damascene-configuration with fully-self-aligned-via (FSAV) reported for first time. At CD~10 nm, AR6 Ru measured is 75% lower than Cu R simulated at AR2. R~33Ω is FSAV of CD bottom of 8.5x12.3 nm^2. Ru line interfaces is good, indicated by thermal shock with delta-R~0 post 1000 h of thermal cycling between -50°C-125°C.

9:55 AM

13-3 Tungsten Interconnect Resistance Reduction Enabling Energy Efficient and High Performance Applications for 2nm Node and Beyond

Gaurav Thareja[1], Ashish Pal[1], Quan Ma[1], Chi Ching[1], Sahil Patel[1], Xingyao Gao[1], Sefa Dag[1], Zhimin Qi[1], Aixi Zhang[1], Shiyu Yue[1], Wei Lei[1], Yi Xu[1], Yu Lei[1], Hao Jiang[1], Shi You[1], Wenkai Zheng[1], Raymond Hung[1], Gregory Costrini[1], Qing Zhu[1], Randy Tran[1], Rohit Gupta[1], Vinod Reddy[1], Pratik B. Vyas[1], Sajjad Hassan[1], Man Ping Cai[1], Gang Shen[1], Zhebo Chen[1], Wenting Hou[1], Jianxin Lei[1], Rongjun Wang[1], Walters Shen[1], Sameer Deshpande[1], Sidney Huey[1], Jianshe Tang[1], Mehul Naik[1], Sree Kesapragada[1], Buvna Ayyagari[1], El Mehdi Bazizi[1], Xianmin Tang[1]
[1]Applied Materials

We present a Tungsten integration scheme for advanced technology nodes using integrated pre-clean, PVD W liner deposition, CVD W gapfill, and CMP process. Electrical results (resistance, reliability) combined with Materials-to-Systems Co-Optimization (MSCO) simulations confirm significant power-performance-area (PPA) improvements, thereby enabling energy efficient, high-performance applications for 2nm technology node and beyond.

10:45 AM

13-4 Heterogeneous Power Delivery for Large Chiplet-based Systems using Integrated GaN/Si-Interconnect Fabric with sub-10 μm Bond Pitch

Haoxiang Ren[1], Krutikesh Sahoo[1], Ziyi Guo[1], Rishi Pugazhendhi[1], Zachary Wong[1], Tianyu Xiang[1], Timothy S. Fisher[1], Subramanian S. Iyer[1]
[1]UCLA CHIPS

We present a wafer-level heterogeneous integration approach connecting GaN-on-Si switches to wafer-scale systems using a segmented highly-granular PDN with a sub-10μm Cu-Cu bond pitch. Additionally, we demonstrate a novel dielet-side PDN that eliminates the need for TSVs and wafer thinning. This work enables large-scale AI/ML systems beyond classical interposer technology.

11:10 AM

13-5 Role of Inter-Layer Dielectric on the Electrical and Heat Dissipation Characteristics in the Heterogeneous 3D Sequential CFETs with Ge p-FETs on Si n-FETs

Seong Kwang Kim[1], Hyeong-Rak Lim[1], Seong Kwang Kim[1], Joonsup Shim[1], Woojin Baek[1], Seongho Kim[1], Youngkeun Park[1], Jaejoong Jeong[1], Jinha Lim[1], Joon Pyo Kim[1], Jaeyong Jeong[1], Bong Ho Kim[1], Dae-Myong Geum[2], Byung Jin Cho[1], Sanghyeon Kim[1]
[1]School of Electrical Engineering, KAIST, Daejeon, [2]School of Electronics Engineering, Chungbuk National University

In this work, we first investigated the electrical and heat dissipation characteristics during the operation of top devices in a 3D sequential CFETs with Ge channel as top devices. These results strongly indicate that ILD thickness is a crucial design parameter for determining device performance within its inherent 3D structure.

11:35 AM
13-6 The Challenges and Solutions of Cu/SiCN Wafer-to-Wafer Hybrid Bonding Scaling Down to 400nm Pitch
Soon Aik Chew[1], Boyao Zhang[1], Joke De Messemaeker[1], Emmanuel Chery[1], Kris Vanstreels[1], Liesbeth Witters[1], Joeri De Vos[1], Sven Dewilde[1], Serena Iacovo[1], Michele Stucchi[1], Koen Van Sever[1], Gerald Beyer[1], Andy Miller[1], Eric Beyne[1]
[1]imec

This paper, we review the current state of W2W bonding technology and discuss recent breakthroughs that have enabled significant scaling. The results show successful control of Cu/SiCN surface topography, precise alignment accuracy, and favorable electrical performance. We analyze the relationship between bonding overlay and contact resistance, yield performance, and reliability.

Session 14: Emerging Device and Compute Technology (EDT) - Emerging devices for AI/Quantum technologies - Part I
9:00 AM, Continental 5
Co-Chairs: Amir Sammak, TNO and Qiming Shao, HKUST

Explosive growth in data intensive applications demands computing schemes that allow large amount of data processing with high bandwidth. Artificial intelligence (AI) and quantum technologies are two potential solutions to address these computing requirements. Emerging devices with their unique properties can be enablers for energy-efficient AI and quantum technologies. Computing-in-memory (CiM) is a promising technique for accelerating the data-intensive artificial intelligence (AI) applications. First paper, reports fabricated and measured 2-layer vertically stacked channel-all-around (CAA)-IGZO 4F2 2T0C cells; and proposes on an ultra-dense and robust 3D eDRAM CiM accelerator with the local-computing scheme. With massive edge devices deployed in the physical world, processing high-resolution images has been a high demanding quest for AI to understand the environment. Second paper demonstrates a monolithically integrated IGZO/CNT hybrid-polarity 2T0C DRAM cell for edge AI applications. Micro-fabricated surface electrode ion traps are a leading platform for achieving the blueprint of quantum information processing. Third paper presents the design, fabrication, and test of ring surface trap on 12-inch wafers with a CMOS process. Frequency multiplication is a nonlinear process that generates high harmonics from base frequency, which has many applications in RF devices and emerging quantum systems. Fourth paper demonstrates the nonlinear spin-wave interaction-induced high harmonic wave that can achieve coherent quantum control of a qubit. Integration of 2D material in silicon microchips is indispensable for emerging computation. Fifth (invited) paper focuses on microchips with pre-patterned CMOS circuits on which the 2D material is deposited at the back-end-of-line (BEOL).

9:05 AM
14-1 30 Mb/mm^2/layer 3D eDRAM Computing-in-Memory with Embedded BEOL Peripherals and Local Layer-wise Calibration based on First-Demonstrated Vertically-Stacked CAA-IGZO 4F^2 2T0C Cell
Wenjun Tang[1], Chuanke Chen[2], Jialong Liu[1], Chunyu Zhang[2], Chen Gu[2], Huazhong Yang[1], Ling Li[2], Xueqing Li[1], Di Geng[2]
[1]Tsinghua University, [2]Institute of Microelectronics of the Chinese Academy of Sciences
This paper, for the first time, reports fabricated and measured 2-layer vertically-stacked channel-all-around (CAA)-IGZO 4F^2 2T0C cells. Based on this area-efficient cell structure, an ultra-dense and robust 3D eDRAM

computing-in-memory (CiM) accelerator with the local-computing scheme, consisting of stacked BEOL memory arrays, BEOL multiplexing peripherals, and FEOL local layer-wise calibration, is proposed. The measurement and evaluation results show that the proposed 3D eDRAM CiM achieves ultra-high memory and computing density up to 30 Mb/mm^2/layer and 50 TOPS/mm^2.

9:30 AM

14-2 Counteractive Coupling IGZO/CNT Hybrid 2T0C DRAM Accelerating RRAM-based Computing-In-Memory via Monolithic 3D Integration for Edge AI

Mingcheng Shi[1], Yanbo Su[1], Jianshi Tang[1], Yijun Li[1], Yiwei Du[1], Ran An[1], Jiaming Li[1], Yuankun Li[1], Jian Yao[2], Ruofei Hu[1], Yuan He[1], Yue Xi[1], Qingwen Li[2], Song Qiu[2], Qingtian Zhang[1], Liyang Pan[1], Bin Gao[1], He Qian[1], Huaqiang Wu[1]
[1]Tsinghua University, [2]Chinese Academy of Sciences

We demonstrate a novel BEOL IGZO/CNT hybrid-polarity 2T0C DRAM cell integrated on our analog RRAM-based M3D platform. Besides incorporating ultra-low-leakage IGZO for write transistor and high-current carbon nanotubes CNTs for read, this hybrid-polarity 2T0C design also enhances the effective sensing window and addresses the charge injection issue through counteractive coupling.

9:55 AM

14-3 CMOS-Fabricated Ring Surface Ion Trap with TSV Integration

Peng Zhao[1,2,3], Yu Dian Lim[2], Hongyu Li[3], Jean-Pierre Likforman[4], Luca Guidoni[4], Lilay Gros Desormeaux[4], Chuan Seng Tan[2]
[1]Interuniversity Microelectronics Centre (IMEC), [2]Nanyang Technological University, [3]Institute of Microelectronics, [4]Université Paris Cité

We present the design, fabrication, and test of ring surface trap on 12-inch wafers with a CMOS process. The design is based on Through Silicon Vias (TSV) interconnects. Up to 200 ions were loaded and cooled; preliminary compensations of electrostatic potential imperfections show that rotational symmetry can be partially restored.

10:45 AM

14-5 On-chip zero-field spin wave frequency multiplier and its application on qubit quantum control

Jiacheng Liu[1], Jiahao Wu[1], Zheyu Ren[1], Sen Yang[1], Qiming Shao[1]
[1]The Hong Kong University of Science and Technology

We demonstrate a 5th harmonic spin-wave frequency multiplier at zero field on a low-damping CoFeB on-chip waveguide. The multiplication process is understood through micromagnetic simulations and detected via the nitrogen-vacancy center. For the first time, we show that the generated high-harmonic wave can drive coherent quantum control of a qubit.

11:10 AM

14-6 Back-end-of-line integration of 2D materials on silicon microchips (Invited)

mario lanza[1], Sebastian Pazos[1], Kaichen Zhu[1], Yue Yuan[1], Yaqing Shen[1], Osamah Alharbi[1], wenwen zheng[1], xixiang zhang[1], Husam Niman Alshareef[1]
[1]King Abdullah University of Science and Technology (KAUST)

In this invited article, we discuss the integration of 2D materials in silicon microchips. We analyze the type of materials and their properties, the main synthesis and manipulation methods, the type of circuits fabricated, the electronic performance achieved, as well as the future challenges and solutions.

Session 15: Focus Session 2: MT - Logic, Memory, Package and System Technologies for Future Generative AI

9:00 AM, Continental 6
Co-Chairs: Suock Chung, SK Hynix and Nanbo Gong, IBM

This focus session extensively covers "the system requirements, technical barriers and solutions including memory technology" for AI computing. The first paper (by Synopsys) explored the emerging trends in generative AI and the role of transformer based neural networks at their core. It shows CNN-optimized hardware accelerators do not effectively scale for transformers. The second paper (by IBM) reported architectural, wafer-scale testing, chip-demo, and hardware-aware training efforts towards Analog Non-Volatile Memory-based accelerators, which offer high-throughput and energy-efficient Multiply-Accumulate operations for the large Fully Connected layers that dominate Transformer-based Large Language Models. The 3rd paper (by Samsung) predicted the direction of change in the structure and function of the memory system in the era of AI computation based on large language models. It comprehensively summarizes the Logic Cores & Memory Convergence (Core Units Position Near or in Memory Computing, PNM-PIM-CIM) method for increasing B/W and minimizing power growth in data movement. The 4th paper (by AMD) emphasized the technical challenges for energy-efficient generative AI and proposed the Near Memory Processor. The 5th paper (by Intel) reported the need for new challenges (2.5D/3D, M3D) in terms of system integration as well as device scaling, in order to improve speed and power or energy efficiency for large computations in the future. The 6th paper (by SK Hynix) reported the importances of HBM and PiM for AI computing. Especially TSV, MR MUF, hybrid bonding, new PKG materials and structural technologies are proposed. The 7th paper (by Micron) introduced 32Gb-NVM memory chip (2 stack FeRAM, 4F2-Poly Si Vertical Gate Tr, PUC architecture) technology, which is a world-largest density RAM with reasonable reliability and performance on CXL interface.

9:05 AM

15-1 Generative AI on a Budget: Processing Transformer-based Neural Networks at the Edge (Invited)

Yankin Tanurhan[1], Pierre Paulin[1], Tom Michiels[1]
[1]Synopsys, Inc.

This paper explores emerging trends in generative AI and the role of transformer-based neural networks at their core. We show how they diverge from conventional CNNs and that CNN-optimized hardware accelerators do not effectively scale for transformers. We introduce the NPX6 NPU and demonstrate its efficient handling of transformer-based models.

9:30 AM

15-2 Design of Analog-AI Hardware Accelerators for Transformer-based Language Models (Invited)

Geoffrey W. Burr[1], Hsinyu Tsai[1], William Simon[2], Irem Boybat[2], Stefano Ambrogio[1], Chung-En Ho[1], Ze-Wei Liou[1], Malte Rasch[3], Julian Buechel[2], Pritish Narayanan[1], Tarl Gordon[4], Shubham Jain[3], Theodore M. Levin[4], Kohji Hosokawa[5], Manuel Le Gallo[2], Hunter Smith[1], Masatoshi Ishii[5], Yasuteru Kohda[5], An Chen[1], Charles Mackin[1], Andrea Fasoli[1], Kaoutar El Maghraoui[3], Ramachandran Muralidhar[3], Atsuya Okazaki[5], Ching-Tzu Chen[3], Martin M. Frank[3], Corey Lammie[2], Athanasios Vasilopoulos[2], Alexander M. Friz[1], Jose Luquin[1], Sean Teehan[4], Ishtiaq Ahsan[4], Abu Sebastian[2], Vijay Narayanan[3]
[1]IBM Research--Almaden, [2]IBM Research--Zurich, [3]IBM Research–T. J. Watson Research Center, [4]IBM Albany NanoTech, [5]IBM Tokyo Research Laboratory

Analog Non-Volatile Memory-based accelerators offer high-throughput and energy-efficient Multiply-Accumulate operations for the large Fully-Connected layers that dominate Transformer-based Large Language Models. We describe architectural, wafer-scale testing, chip-demo, and hardware-aware training efforts towards such accelerators, and quantify the unique raw-throughput and latency benefits of Fully- (rather than Partially-) Weight-Stationary systems.

9:55 AM

15-3 The Era of Generative Artificial Intelligence: In-Memory Computing Perspective (Invited)

Kyomin Sohn[1], Shin-haeng Kang[1], Sukhan Lee[1]
[1]Samsung Electronics

With the emergence of large language models, in-memory computing is gaining attention to solve memory bottlenecks and enhance energy efficiency. This paper provides an explanation of the key concepts of in-

memory computing and presents the performance of processing-in-memory technology when applied to the representative large language models, GPT.

10:45 AM

15-4 Innovations For Energy Efficient Generative AI (Invited)

Samuel Naffziger[1]
[1]AMD

The explosion in the capabilities of generative AI are much discussed, as is the unprecedented amount of compute and energy required train and serve these models. This paper will discuss the innovations required to meet the compute needs of AI while staying within environmental and economic limits of energy consumption.

11:10 AM

15-5 Beyond Exascale: A paradigm shift for AI and HPC (Invited)

Wilfred Gomes[1]
[1]Intel

The need for High-Performance Computing (HPC) and Artificial Intelligence (AI) has given rise to new class of Exaflop computers to solve fundamental problems. The development of PVC introduced the GPU, Advanced 3D packaging, Large Caches, Thermals and Power Delivery to build an Exaflop System. We build upon these innovations and introduce the CPU+GPU architecture leveraging next Generation Process and Advanced Packaging, 3D monolithic Compute + memory, Photonics, Wafer/Panel Scale integration with Glass to get beyond Exascale.

11:35 AM

15-6 Advanced Packaging Technologies in Memory Applications for Future Generative AI Era (Invited)

KI-ILL MOON[1], Ho-Young Son[1], Kangwook Lee[1]
[1]SK Hynix

It is expected that memory usage will exponentially increase according to the explosive interest in generative AI and its expanded application. Along with this industrial trend, the demand for memory products with high bandwidth, high capacity, and better power efficiency is increasing. In this paper, we would like to introduce key packaging technology of a high bandwidth memory (HBM) and its future challenges which SK Hynix has led its technology as world 1st and world best performance.

12:00 PM

15-7 NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads (Invited)

Nirmal Ramaswamy[1], Alessandro Calderoni[1], John Zahurak[1], Giorgio Servalli[1], Ashnoita Chavan[1], Sameer Chhajed[1], Murali Balakrishnan[1], Mark Fischer[1], Matthew J Hollander[1], Devanarayanan Perinthatta Ettisserry[1], Albert Liao[1], Kamal Karda[1], Matthew Jerry[1], Marcello Mariani[1], Angelo Visconti[1], Beth R Cook[1], Bryce D Cook[1], Duane Mills[1], Alessandro Torsi[1], Chandra Mouli[1], Erik Byers[1], Mark Helm[1], Steve Pawlowski[1], Shigeru Shiratake[1], Naga Chandrasekaran[1]
[1]Micron

NVDRAM is the world's first dual-layer, high-performance, high-density (32Gb) and non-volatile ferroelectric memory technology. NVDRAM uses ultra-scaled ferroelectric capacitor as memory cell and a dual gated, stackable, polycrystalline silicon transistor access device. To achieve high memory density, two memory layers utilizing a $4F^2$ architecture with 48nm pitch are fabricated above CMOS circuitry. Full package yield is demonstrated from -40°C to 95°C along with 10yr reliability (endurance and retention). NVDRAM utilizes the LPDDR5 command protocol and system compatibility is successfully demonstrated using a commercial development platform. NVDRAM achieves a bit density of $0.45Gb/mm^2$, higher than Micron's industry-leading 1b planar DRAM technology.

Session 16: Modeling and Simulation (MS) - First Principles Transport Modeling for Logic, Memory, and Optical Devices
9:00 AM, Continental 7-9
Co-Chairs: Roza Kotlyar, Intel Corporation and Tzer-Min Shen, TSMC

This session focuses on advanced modeling techniques applied to transport in devices ranging from Si logic, novel ferroelectric memory to optical diodes. The first paper by Phil-Hun Ahn and Sung-Min Hong from Gwangju Institute of Science and Technology, Korea, introduces a novel geometry scattering approach to describe transport in Silicon scaled devices that have nonuniform cros-sections. The second paper by Zirui Wang et al. from School of Integrated Circuits, Peking University, China, provides ab-initio insights into the mechanism of hot carrier degradation versus wafer orientation for NMOS and PMOS. The third paper by H. Lee and M. Shin from Korea Advanced Institute of Science and Technology, South Korea, combines quantum transport techniques with phase field description to capture effects of polar topological states on device characteristics of ferroelectric based STO-PTO-STO capacitors and transistors. The fourth paper by J. Cao from Integrated Systems Laboratory, ETH Zurich, Switzerland, applies ab-initio quantum transport to study optical properties of InAs photo-diodes. The session concludes with the invited paper by S. Pellegrini et al. from STMicroelectronics, United Kingdom, which reviews first-principles-based simulation for design and trade-offs for Single-Photon Avalanche Diodes (SPADs).

9:05 AM
16-1 Geometric scattering describing mode-coupling effects in non-uniform cross-sections for non-equilibrium Green's function and multi subband Boltzmann transport equation solvers
Phil-Hun Ahn[1], Sung-Min Hong[1]
[1]Gwangju Institute of Science and Technology

The non-uniformity of device cross-sections is modeled as a geometric scattering in advanced microscopic transport solvers. With the proposed geometric scattering, the carrier density including the mode-coupling effects can be accurately calculated in the NEGF simulation. The proposed approach allows the MSBTE simulation for MOSFETs with non-uniform cross-sections.

9:30 AM
16-2 New Insights into the Interface Trap Generation during Hot Carrier Degradation: Impacts of Full-band Electronic Resonance, (100) vs (110), and nMOS vs pMOS
Zirui Wang[1], Haoran Lu[1], Zixuan Sun[1], Cong Shen[1], Baokang Peng[1], Wen-Feng Li[2], Yongkang Xue[3], Da Wang[3], Zhigang Ji[3], Lining Zhang[4], Xiangwei Jiang[5], Yue-Yang Liu[2], Runsheng Wang[1,1], Ru Huang[1]
[1]Peking University, [2]Institute of Semiconductors, Chinese Academy of Sciences, [3]Shanghai Jiao Tong University, [4]Peking University, Shenzhen, [5]National Natural Science Foundation of China

The physics of interface trap generation are revealed, by using full-band distribution of H atom electronic resonance states in Si-H bond at Si/SiO2 interface. The idea is verified by TDDFT calculations. The hot carrier degradation can be well modeled to cover a broad range of technologies and stress conditions, due to the multiple peaks found in the full-band resonance states, and a TCAD simulation flow is proposed. The model is experimentally validated, from classic region (130nm Planar) to advanced region (16/14nm FinFET) and extendable to GAA, covering both (100) & (110) and n & p channels with various Vgs/Vds bias conditions.

9:55 AM
16-3 Three-Dimensional Phase-Field based Quantum Transport Simulations of Polar Topological States
Hyeongu Lee[1], Mincheol Shin[1]
[1]Korea Advanced Institute of Science and Technology (KAIST)

We present a 3D phase field-based quantum transport simulation framework for a polar topological state in thin film capacitor and FEFETs. Our findings include: (i) manipulation of polar topological states using electrical

pulses and (ii) control of topological number through pulse width variations for the functionality of potentiation and depression.

10:20 AM
16-4 *Ab initio* quantum transport simulations of InAs avalanche photo-diodes within the *GW* approximation
Jiang Cao[1], Alexandros Nikolaos Ziogas[1], Leonard Deuschle[1], Qian Ding[1], Nicolas Vetsch[1], Anders Winka[1], Vincent Maillou[1], Alexander Maeder[1], Mathieu Luisier[1]
[1]ETH Zurich

A self-consistent quantum transport simulation framework incorporating electron-electron and electron-photon interactions from first-principles is presented. It relies on density functional theory, NEGF formalism, and the *GW* approximation to account for many-body effects. We demonstrate that this approach can deliver accurate bandgaps and captures impact-ionization, light absorption, and photon-induced avalanche physics.

10:45 AM
16-5 Simulation in action: the application of modelling to SPAD architecture design (Invited)
Sara Pellegrini[1], Isobel Nicholson[1], Remi Helleboid[1], Bastien Mamdy[1], Giulio Forcolin[1], Mohammed Al-Rawhani[1], Christel Buj[1], Guillaume Marchand[1], Dominique Golanski[1], Gabriel Mugny[1], Raul Andres Bianchi[1], Bruce Rae[1], Denis Rideau[1]
[1]STMicroelectronics

We review the many considerations required to design a SPAD from first principles and illustrate the complex flow of simulations and tradeoffs required to create a pixel that's performance reaches the level required by the application on all figures of merit.

Session 17: Sensors, Mems, and Bioelectronics (SMB) - MEMS for Communication & Sensing
9:00 AM, Imperial A
Co-Chairs: Marc Faucher, CNRS-IEMN and Philip Feng, University of Florida

This session is focused on RF MEMS technologies and includes five papers that highlight some of the latest advances at the frontiers of RF MEMS and acoustic resonators, filters, oscillators, sensors and biosensors encompassing representative technical progress in design, advanced micro/nanofabrication, integration, characterization, and emerging applications in communication, timing, and sensing. The first paper is from Institute of Microelectronics, A*STAR (Singapore), presenting a 15GHz filter using AlScN (Aluminum Scandium Nitride), BAW (bulk acoustic wave) resonator and filter technology for acoustic filters for emerging high frequency communication in the mm-wave spectrum. The second paper is from National Tsing Hua University, Taiwan, reporting a MEMS-based quartz oscillator, using a selective 3rd overtone oscillation and demonstrating low acceleration sensitivity (G-sensitivity) and a reduced footprint, for 5G wireless communications. The third paper is from National Tsing Hua University, Taiwan and demonstrates a MEMS oscillator with low close-in phase noise and low power which is important for wireless communications, especially mobile applications. The fourth paper is from University of Florida, Gainesville, describing MoS2 nanoelectromechanical systems (NEMS). The demonstrated devices are vibrating channel transistors with graphene enhanced contacts, where the unconventional electrical and mechanical properties enable to self-detect 32 MHz electromechanical resonances and also their own thermomechanical motion. The fifth paper is from CNRS-LAAS and Georgia Tech University, that proposes different porous silicon membranes technologies to achieve on-chip microfluidic functions, like protein concentration. The key aspect lies in strategies to achieve lateral architectures on SOI, potentially paving the way for a porous silicon-based technology to handle all aspects of analytical biology, from sample preparation to biosensing.

9:05 AM
17-1 Thin $Sc_{0.2}Al_{0.8}N$ Film Based 15GHz Wideband Filter: Towards mmWave Acoustic Filters

Xinghua Wang[1], Chen Liu[1], Ying Zhang[1], Wenjia Yang[1], You Qian[1], Peng Liu[1], Zhan Jiang Quek[1], Yan Hong[1], Eugene Yi Zhun Woo[1], Huamao Lin[1], Qingxin Zhang[1], Peter Hyun Kee Chang[1], Yao Zhu[1]
[1]Institute of Microelectronics, A*STAR

In this work, 200 mm wafer-level 15 GHz bulk acoustic wave (BAW) resonators and filters have been demonstrated based on 90nm thin $Sc_{0.2}Al_{0.8}N$ film. The fabricated filters have demonstrated a fractional bandwidth of ~ 10%. The results indicate the possibility of ScAlN-based BAW technology going beyond 10 GHz towards mmWave frequency.

9:30 AM
17-2 A Selective Overtone MEMS-based Quartz Oscillator with Low Acceleration Sensitivity
Chin-Yu Chang[1], Po-Cheng Hsieh[1], Chun-Wei Yao[1], Chien-Cheng Yang[2], Sheng-Shian Li[1]
[1]National Tsing Hua University, [2]Taitien Electronics Company Ltd.

This study investigates a MEMS-based quartz oscillator simultaneously with selective 3rd-overtone oscillation and low acceleration sensitivity. We implement (i) aspect-ratio design through acoustic wave engineering to mitigate the fundamental thickness shear mode while accentuating its 3rd-overtone and (ii) folded structure to alleviate inertia induced stress, thus realizing low acceleration sensitivity.

9:55 AM
17-3 A Low Phase Noise Piezoelectric MEMS Oscillator with Low Power Consumption
Pang-Che Lo[1], Wei Lin[1], Sheng-Shian Li[1]
[1]National Tsing Hua University

This work demonstrates piezoelectric MEMS oscillator in 17.55 MHz. A record low phase noise of piezoelectric MEMS oscillator is measured, −136 dBc/Hz at 1 kHz offset with 154 μW power consumption in air. −137 dBc/Hz at 1 kHz offset with 148 μW power consumption in vacuum.

10:20 AM
17-4 High-Performance Monolayer and Bilayer MoS_2 Vibrating Channel Transistors for Ultrasensitive Drain-Source Current Readout of Resonant Motion
S M Enamul Hoque Yousuf[1], Philip X.-L. Feng[1]
[1]University of Florida

We demonstrate high-performance monolayer (1L) and bilayer (2L) MoS_2 vibrating channel transistors (VCTs), and for the first time, directly read out the nm-scale motion of the MoS_2 VCTs by probing the small-signal drain-source current (i_{DS}). 1L-MoS_2 VCT exhibit**s** on-current I_{on} = 0.1μA/μm at small V_{DS} = 0.1V, on-off ratio $I_{on}/I_{Off} > 10^5$, and transconductance g_m = 13nS/μV. 2L-MoS_2 VCTs demonstrate I_{on} = 0.2μA/μm at V_{DS}=0.1V, $I_{on}/I_{Off} > 10^5$, and g_m = 38nS/μV. We have achieved very high electron mobility (μ_E ~492 $cm^2/(V{\cdot}s)$) in the 2L-MoS_2 VCT. We resolve channel current down to **6**pA by directly measuring i_{DS} of radio-frequency VCTs.

10:45 AM
17-5 On-chip sample preparation and biosensing: Can porous silicon membranes do it all? ((nvited)
Thierry Leichle[1], Yingning He[2], Douglas Silva de Vasconcellos[2], Eric Imbernon[2], David Bourrier[2]
[1]Georgia Tech-CNRS, [2]LAAS-CNRS

We present a strategy for the monolithic integration of multiple porous silicon membranes with tunable properties in planar microfluidics, thus paving the way towards the use of porous silicon to achieve all the functions involved in the bioanalytical process, from sample preparation to biosensing, on a single chip.

Session 18: Reliability Of Systems and Devices (RSD) - Advances in Ferroelectric Devices
9:00 AM, Imperial B
Co-Chairs: Michael Waltl, TU Wien and Brecht Truijen, IMEC

This session includes five papers that describe recent advances in ferroelectric devices. The first paper provides evidence that ferroelectric fatigue and recovery in doped-HfO2 capacitors are dominated by the redistribution of oxygen vacancies. The session continues with two papers discussing recovery strategies for FeFETs. The first of these two demonstrates a significant improvement in endurance cycles by optimized recovery pulses, together with a nearly zero loss in memory window per recovery period. The following paper shows that IL scavenging reduces operating voltage and improves endurance/retention characteristics. The fourth paper proposes a novel PUF based on a 10×10 FeFET array, delivering high security, reliability, and reconfigurability. The session concludes by looking at temperature dependence in ferroelectric devices. Paper five demonstrates how existing Fe-TFT crossbar arrays can sense temperature and detect run-time thermal fluctuations, enabling the Fe-TFT array to adjust bias conditions and operate reliably over various temperatures self-adaptively.

9:05 AM

18-1 Physical Origin of Recovable Ferroelectric Fatigue and Recovery for Doped-HfO_2: Toward Endurance Immunity

Jiajia Chen[1], Haoji Qian[1], Hongrui Zhang[1], Rongzong Shen[1], Gaobo Lin[1], Jiani Gu[1], Chengji Jin[1], Miaomiao Zhang[1], Huan Liu[1], Yan Liu[2], Xiao Yu[1], Genquan Han[1,2]
[1]Research Center for Intelligent Chips and Devices, Zhejiang Lab, [2]School of Microelectronics, Xidian University

We have experimentally and theoretically demonstrated that the recovery of remnant polarization (Pr) degradation for ferroelectricity in doped-HfO_2 under high electric fields is not dominated by charge detrapping effects, but rather the redistribution of oxygen vacancies (V_o). The Pr degradation under low electric field is mainly due to the non-uniform distribution caused by migration in the in-plane direction. The two-dimensional distribution of V_o characterized by EELS, first principles calculation, and phase-field model calculation results strongly support the proposed mechanism. Moreover, with increased cycles of fatigue-recovery, the device approaches an infinitely stable state, which seems to be a much more meaningful discovery.

9:30 AM

18-2 Robust Recovery Scheme for MFIS-FeFETs at Optimal Timing with Prolonged Endurance: Fast-Unipolar Pulsing (100 ns), Nearly Zero Memory Window Loss (0.02 %), and Self-Tracking Circuit Design

Cheng-Hung Wu[1], Jay Liu[1], Xun-Ting Zheng[1], Yi-Ming Tseng[1], Masaharu Kobayashi[2], Vita Pi-Ho Hu[1], Chun-Jung Su[3]
[1]National Taiwan University, [2]The University of Tokyo, [3]National Yang Ming Chiao Tung University

A robust recovery scheme for MFIS-FeFET is demonstrated. A 100-ns fast-unipolar pulsing treatment at optimized timing prolongs endurance cycles by a factor of 10^2, featuring a MW loss of 0.02% per recovery and ultra-low recovery-induced time loss ratio of 5×10^{-5}%. A self-tracking circuit is designed to automatically trigger the recovery.

9:55 AM

18-3 IL Scavenging and Recovery Strategies to Improve the Performance and Reliability of HZO-Based FeFETs

Bong Ho Kim[1], Seong Kwang Kim[1], Song-Hyeon Kuk[1], Yoon-Je Suh[1], Jaeyong Jeong[1], Joon Pyo Kim[1], Dae-Myeong Geum[2], Sanghyeon Kim[1]
[1]KAIST, [2]Chungbuk National University

We investigated the effects of interfacial layer scavenging and $HfZrO_x$ (HZO) scaling on the performance and reliability of HZO-based ferroelectric field-effect transistors (FeFETs). IL scavenging effectively reduced operating voltage and improved endurance/retention characteristics. The sub-loop operation and recovery strategies are proposed to extend the endurance characteristics of FeFETs. The results provide insights into the degradation/recovery mechanisms of gate stacks in FeFETs and highlight the importance of recovery speed and controlled IL.

10:45 AM

18-4 A Novel FeFET Array-Based PUF: Co-optimization of Entropy Source and CRP Generation for Enhanced Robustness in IoT Security

Hanyong Shao[1], Yuejia Zhou[1], Weiqin Huang[1], Chang Su[1], Zhiyuan Fu[1], Wenpu Luo[1], Kechao Tang[1], Ru Huang[1]
[1]Peking University

In this work, we propose a novel strong PUF based on a 10×10 FeFET array, delivering high security, reliability, and reconfigurability. For the first time, the entropy source and CRP generation of PUF are co-optimized for robustness. As a result, our approach reduces the accuracy of ML attacks by 20% compared to RRAM PUF, while keeping the raw bit error rate (BER) down to 1.7% at 100°C. Due to the high endurance of FeFETs, the capacity of reconfigurability reaches 1×10^8.

11:10 AM

18-5 Defying Temperature: Reliable Compute-in-Memory in Monolithic 3D using BEOL Ferroelectric TFT

Swetaki Chatterjee[1,2], Shubham Kumar[1,2], Athira Sunil[3], Sourav De[3], David Lehninger[3], Michael Jank[4], Thomas Kämpfe[3], Yogesh Singh Chauhan[1], Hussam Amrouch[5,6][1]Indian Institute of Technology Kanpur, [2]University of Stuttgart, [3]Fraunhofer IPMS, [4]Fraunhofer IISB, [5]MIRMI, Technical University of Munich, [6]Chair of AI Processor Design, Technical University of Munich

This work presented a novel method to overcome the temperature-induced accuracy degradation caused in monolithic 3D chips that use Fe-TFTs. It uses a novel temperature sensing and bias-optimization schemes with minimal overhead costs. Further, we presented temperature measurements from fabricated Fe-TFTs, comprehensive thermal modeling and DNN accuracy investigations.

Career Lunch

12:20 PM, Grand Ballroom B

In this IEDM Career Luncheon, the IEDM Executive Committee invites student conference attendees, aspiring professionals, and the IEDM community at-large to join invited eminent speakers in a casual, buffet lunch setting to discuss topics related to their careers and their experience in the semiconductor and system community. We encourage the audience to attend this luncheon and engage with the distinguished speakers as they seek answers to their career development questions and the overall evolution of the semiconductor ecosystem.

Career Luncheon

Tuesday, December 10, 12:25 - 2:10 PM
Grand Ballroom B
Moderator: Jennifer Zhao, President and CEO of ams OSRAM USA Inc.

Speakers: Isabelle Ferain, VP of Technology Development of Globalfoundries
Ilesanmi Adesida, Provost and Acting President at Nazarbayev University in Kazakhstan

In this IEDM Career Luncheon, the IEDM Executive Committee invites student conference attendees, aspiring professionals, and the IEDM community at-large to join eminent speakers in a casual, buffet lunch setting to discuss topics related to their careers and their experience in academia and semiconductor industry. Our distinguished speakers this year, Dr. Isabelle Ferain VP of Technology Development of Globalfoundries and Prof. Ilesanmi Adesida, Provost and Acting President at Nazarbayev University in Kazakhstan, will share their perspectives on the future of semiconductor technology. The luncheon will be moderated by Jennifer Zhao, President and CEO of ams OSRAM USA Inc. We encourage the audience to attend this luncheon and engage with the distinguished speakers as they seek answers to their career development questions and the overall evolution of the semiconductor ecosystem.

2023 IEEE Cledo Brunetti Award

To: John Robertson - "*For theoretical contributions to the integration of high-k oxides on semiconductors*".

2023 IEEE Frederik Philips Award

To: Omkaram (Om) Nalamasu - "*For leadership in research and development of semiconductor materials, processes, and equipment*".

2023 IEEE Kiyo Tomiyasu Award

To: Tim Böscke - "*For contributions to the discovery of ferroelectricity in hafnium-based oxides*".

Session 19: Focus Session 3: ALT - Focus Session - 3D Stacking for Next-Generation Logic & Memory by Wafer Bonding and Related Technologies
2:15 PM, Grand Ballroom A
Co-Chairs: You-Seok Suh, Qualcomm and Bich-Yen Nguyen, SOITEC
3D stacking of integrated circuits is required to meet the demands of ever-growing computing and AI workloads while realizing a PPAC benefit (performance, power, area and cost). The first three papers present 3D integration, exploring innovation in material/process/tool and design with extensive implementation of DTCO and STCO. The bottleneck of the back-end of the line interconnects is also addressed with the backside contact for the power distribution network, backside contact, and thermal dissipation. The last three papers cover low-temperature wafer bonding and low-temperature device integration, which are key processes for Complementary FET or 3D-IC stacking.

2:20 PM
19-1 Process Innovations for Future Technology Nodes with Back-Side Power Delivery and 3D Device Stacking (Invited)
Mauro Javier Kobrinsky[1], Joseph D Silva[1], Ehren Mannebach[1], Shaun Mills[1], Makram Abd El Qader[1], Olajuyigbe Adebayo[1], Nischal Radhakrishna[1], Madeleine Beasley[1], Seda Cekli[1], Jasmeet Chawla[1], Sunny Chugh[1], Evan Clinton[1], Anindya Dasgupta[1], Umang Desai[1], Eleonora De Re[1], Gilbert Dewey[1], Trenton Edwards[1], Valur Gudmundsson[1], Clifford Engel[1], Rohit Galatage[1], Jeffrey Hicks[1], Brian Krist[1], Rishabh Mehandru[1], Inanc Meric[1], Patrick Morrow[1], Debaleena Nandi[1], Pratik Patel[1], Marko Radosavljevic[1], Rahul Ramamurthy[1], Dipanjan Samanta[1], Leah Shoer[1], Anthony St Amour[1], Li Huey Tan[1], Sukru Yemenicioglu[1], Xinning Wang[1], Tahir Ghani[1]
[1]Intel

Process Innovations for Future Technology Nodes with Back-Side Power Delivery and 3D Device Stacking

2:45 PM
19-2 Backside Power Delivery: Game Changer and Key Enabler of Advanced Logic Scaling and New STCO Opportunities (Invited)
Anabela Veloso[1], Bjorn Vermeersch[1], Rongmei Chen[1], Philippe Matagne[1], Marie Garcia Bardon[1], Geert Eneman[1], Kateryna Serbulova[1], Odysseas Zografos[1], Shih-Hung Chen[1], Giuliano Sisto[1], Anne Jourdain[1], Hiroaki Arimura[1], Barry OSullivan[1], An De Keersgieter[1], Geert Hellings[1], Eric Beyne[1], Naoto Horiguchi[1], Julien Ryckaert[1]
[1]Imec

BSPDN is an innovative and game changer approach for on-chip power delivery, key for supporting scaling roadmaps. With no detrimental N/PMOS impact from BS processing demonstrated, this concept can also allow new device engineering opportunities and expand towards a more optimum use of both wafer sides for enhanced system performance.

3:10 PM

19-3 Thermal dissipation in stacked devices (Invited)
Wei-Yen Woon[1], Sam Vaziri[1], Che-Chi Shih[1], Isha Datye[1], Mohamadali Malakoutian[2], James Hsu[1], Ku-Feng Yang[1], Jhih-Rong Huang[1], Tzer-Min Shen[1], Srabanti Chowdhury[2], Xinyu Bao[1], Sandy Szuya Liao[1]
[1]Taiwan Semiconductor Manufacturing Company, [2]Stanford University

In this paper, we present thermal dissipation challenges in three dimensional (3D) stacked devices and discuss strategies to tackle these issues through innovations in materials, integrations, and designs. Back-end-of-line (BEOL) compatible aluminum nitride (AlN) and diamond are evaluated and found to be promising dielectric materials to improve thermal dissipation in 3D stacked devices. Insertion of phonon dispersion matched bridging layers is proposed to solve the thermal boundary resistance issue. We also propose a manufacturing compatible in-line metrology for monitoring the thermal conductivity (κ) and heat dissipation characteristics.

4:00 PM
19-4 Ultimate Layer Stacking Technology for High Density Sequential 3D Integration (Invited)
Ionut Radu[1], Bich-Yen Nguyen[1], Cheng-Hung Chang[1], Cesar Roda Neve[1], Gweltaz Gaudin[1], Guillaume Besnard[1], Anne Vandooren[2], Virginie Loup[3], Perrine Batude[3], Naoto Horiguchi[2]
[1]Soitec, Bernin, France, [2]imec, Leuven, Belgium, [3]CEA-Leti, Université Grenoble Alpes, F-38000 Grenoble, France

Wafer-level stacking technology providing a ultra-thin and single-crystalline silicon film onto a device wafer is reported in this paper. Combining with low temperature device processing, the sequential manufacturing of 3D devices is demonstrated. In this paper we report the first-time demonstration of Smart Cut layer stacking below 350°C.

4:25 PM
19-5 CMOS Directly Bonded to Array (CBA) Technology for Future 3D Flash Memory (Invited)
Masayoshi Tagami[1]
[1]Kioxia Corporation

In this work, CMOS directly bonded to array (CBA) technology is applied to 3D flash memory. As a result, CMOS and cell performance can be improved, and further 2D and 3D scaling can be achieved. CBA technology is essential to realize PPAC goals for future 3D flash memory.

4:50 PM
19-6 Wafer Bonding as Next Generation Scaling Booster (Invited)
Paul Lindner[1], Tobias Wernicke[1], Thomas Uhrmann[1], Markus Wimplinger[1]
[1]EVG

Latest technology trends, focus products and related requirements in the semi-conductor industry are being reviewed and latest direct bonding approaches and their features are introduced. Latest developments, improvements, relevant data as well as roadmap looking to the next years is being presented.

Session 20: Optoelectronics, Displays, and Imaging Systems (ODI) - Emerging Photodetectors
2:15 PM, Continental 1-3
Co-Chairs: Jamie Phillips, University of Delaware and Rainer Minixhofer, AMS OSRAM

This session includes 5 papers that describe recent developments in the area of emerging photodetectors spanning from MIR to the DUV spectral range and from group IV and III-V sensors to organic detectors. The first paper by KAIST presents a fully CMOS compatible Ge on Insulator platform for detection of wavelengths beyond 4 µm. The second paper by KIST presents a new record low jitter SPAD device integrated into a CIS process technology covering a spectral range of visible up to NIR. The third paper by KAIST shows a wavelength tunable detection device combining optical gratings and phase-change materials reaching wavelengths up to 1700 nm. The next paper by the University of Science and Technology of China reports a dual function tunable emitter and NIR photodetector combination based on III-V GaN/AlGaN nanowires on

silicon. The last (invited) paper gives an overview on the next generation of sustainable organic photodetectors and emitters.

2:20 PM
20-1 Fully CMOS-Compatible Room-Temperature Waveguide-Integrated Bolometer Based on Germanium-on-Insulator Platform at Mid-Infrared Operating Beyond 4 μm
Joonsup Shim[1], Jinha Lim[1], Inki Kim[1], Seong Kwang Kim[1], Seung-Yeop Ahn[1], Juhyuk Park[1], Jaeyong Jeong[1], Bong Ho Kim[1], Seunghyeon Lee[2], Jihwan An[3], Dae-Myeong Geum[4], Sanghyeon Kim[1]
[1]School of Electrical Engineering, Korea Advanced Institute of Science & Technology (KAIST), Daejeon, [2]Department of Manufacturing Systems and Design Engineering, Seoul National University of Science and Technology, Seoul, [3]Department of Mechanical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, [4]School of Electronics Engineering, Chungbuk National University, Cheongju

We present the first demonstration of a fully CMOS-compatible, room-temperature waveguide-integrated bolometer operating beyond 4 μm. It utilizes heavily doped Ge for heat generation and H_2 plasma-treated TiO_2 film for thermal-to-electrical conversion. It achieves high performance with -1.911 %/K TCR and -22.25 %/mW sensitivity, opening new possibilities for ultra-wide mid-infrared applications.

2:45 PM
20-2 Back-Illuminated SPAD in 40 nm CIS Technology Achieving 56 ps Timing Jitter With 15 V Breakdown Voltage for Short/Mid-Range LiDAR Applications
Eunsung Park[1,2], Doyoon Eom[1], Joo-Hyun Kim[1], Hyuk An[3], Suhyun Yi[3], Kyung-Do Kim[3], Jongchae Kim[3], Hoon-Sang Oh[3], Woo-Young Choi[2], Myung-Jae Lee[1]
[1]Korea Institute of Science and Technology (KIST), [2]Yonsei University, [3]SK hynix Inc.

We present back-illuminated single-photon avalanche diodes based on stacked 40 nm CIS technology. With doping engineering, it achieves dark count rate of 15 cps/μm2, timing jitter of 97 ps, and excellent photon detection probability of 60% at 905 nm and 44% at 940 nm with the 2.5 V excess bias.

3:10 PM
20-3 Wavelength-tunable grating-resonance InGaAs narrowband photodetector with infrared optical PCM, antimony triselenide (Sb_2Se_3)
Junho Jang[1], Il-Suk Kang[2], Yeon-Wha Oh[2], Sanghee Jung[2], Huijae Cho[2], Sanghyeon Kim[1,1]
[1]School of electrical engineering, KAIST, [2]National Nanofab Center (NNFC)

We successfully fabricated a wavelength-tunable grating-resonance narrowband photodetector (PD) array by wafer bonding of the InGaAs PD layer onto the Si grating and depositing of the wavelength-tuning PCM (Sb_2Se_3) layer on the pixels. Through measurements, we demonstrated excellent wavelength selectivity, high narrowband detection performance, and distinct peak shifts.

3:35 PM
20-4 Highly Responsive Broadband (250~1000 nm) DUV-NIR Photodetector and Tunable Emitter Enabled by Ⅲ-Ⅴ Nanowire on Silicon for Integrated Photonics
Huabin Yu[1], Rui Wang[1], Shudan Xiao[1], Lan Fu[2], Haiding Sun[1]
[1]University of Science and Technology of China, [2]The Australian National University

We proposed a bias-controlled, dual-functional broadband diode enabled by constructing the GaN nanowire-on-Si platform. This device showcases the capability of bias-controlled switchable operation modes, including extreme-broadband photodetectors, narrowband photodetectors, and light-emitting diodes. Various applications including multicolor imaging, filterless color discrimination, and DUV/NIR visualization systems have been explored.

4:00 PM
20-5 Advances in Organic Photodetectors (Invited)

Lionel Hirsch[1], Chloé Dindault[2], Marcin Kielar[3], Gilles H Roche[2], Sylvain Chambon[1], Martial LEYNEY[1], Guillaume Wantz[4]
[1]CNRS/Univ. Bordeaux, [2]Univ. Bordeaux, [3]University of Queensland, [4]Bordeaux INP

In this presentation, we thoroughly discuss organic semiconductors and their role in printing technologies to manufacture the next-generation of sustainable optoelectronic devices. Focusing on organic photodetectors (OPDs), we study multidimensional factors affecting the device impact on the environment. Low-temperature processing and solution-processed printing technologies strongly reduce the environmental footprint of OPDs as compared to inorganic photodetectors. That being said, there is still room to further improve their sustainability by using polymers with simplified synthesis steps and non-halogenated solvents, as well as by using novel methodologies of light detection requiring simple instrumentation.

Session 21: Memory Technology (MT) - RRAM and OTS selected crossbar arrays
2:15 PM, Continental 4
Co-Chairs: Swati Saha, Infineon and Andrea Redaelli, ST Microelectronics

This session has 7 papers on recent advances from RRAM and OTS selected crossbar arrays. The 1st RRAM paper from Tsinghua University implements a new algorithm scheme “COPS” to improve the program efficiency. The 2nd paper from Peking University shows promising results for RRAM using STI less dynamic gate technique with very high memory density and good device performance. The final RRAM paper from TSMC shows promising results on 12nm FFC scaled from 28nm RRAM with insights on write algorithm to compensate process variations in 12nm FFC technology. The second part of this session is related to the ovonic threshold switching selector and related crossbar arrays. The 4th paper is, in fact, an invited paper authored by Micron and it describes the realization of the 3DXpoint, by coupling the OTS selector with the PCM. Scaling opportunities using OTS-only as a memory element is also discussed (SXM). The 5th paper by TSMC is focused on the usage of the OTS selector with STT-MRAM: a comprehensive study is presented paving the way for 1S1R application in embedded memory arrays. The last two papers of the session concern the usage of OTS as self-selecting memory: the 6th paper (POSTECH) is mainly focused on material optimization to maximize device performances while the 7th paper (by Samsung) focuses on the realization of a 64 Gb 16nm dense array showing promising performance for a future exploitation of this technology.

2:20 PM
21-1 COPS: An Efficient and Reliability-Enhanced Programming Scheme for Analog RRAM and On-Chip Implementation of Denoising Diffusion Probabilistic Model
Zhixing Jiang[1], Yue Xi[1], Jianshi Tang[1], Yuyao Lu[1], Ruihua Yu[1], Ruofei Hu[1], Qi Hu[1], Bin Gao[1], He Qian[1], Huaqiang Wu[1]
[1]Tsinghua University

This work develops an efficient and reliability-enhanced programming scheme for analog RRAM, named **C**onductance and **O**peration dependent **P**rogramming **S**cheme (COPS). The advantage of COPS was verified on different RRAM materials stacks by large array-level tests and also on-chip implementations of three representative AI tasks.

2:45 PM
21-2 A Logic-Process Compatible RRAM with 15.43 Mb/mm^2 Density and 10years@150°C retention using STI-less Dynamic-Gate and Self-Passivation Sidewall
Qishen Wang[1], Yuhang Yang[1], Zongwei Wang[1], Shengyu Bao[1], Jingwei Sun[1], Linbo Shan[1], Lin Bao[1,2], Yi Gao[1], Haisu Zhang[1], Yaotian Ling[1], Wuzhi Zhang[3], Yansheng Wang[3], Yimao Cai[1], Ru Huang[1]
[1]Peking University, [2]Beijing University of Posts and Telecommunications, [3]Shanghai Huali Integrated Circuit Corporation

We have demonstrated the STI-less dynamic-gate technique with self-passivation sidewall enhanced RRAM cells on commercial 40nm CMOS production platform achieving record-density of 15.43 Mb/mm^2 and high-

retention of 10years@150°C. Through DTCO, significant improvements in key characteristics are verified at wafer and chip level including memory window, uniformity, retention, and MLC>3bit.

3:10 PM

21-3 Emerging Memory RRAM Embedded in 12FFC FinFET Technology for Industrial Applications

Chun-Yu Wu[1], Chang-Feng Yang[1], Chih-Wei Lai[1], Yu-Tien Wu[1], Ta-Chun Chien[1], Ming-Han Yang[1], Ming-Ta Yang[1], Yu-Neng Kao[1], Chih-Lin Cheng[1], Chia-Yu Wang[1], H. W. Tseng[1], Yu-Der Chih[1], Wen-Ting Chu[1], Arthur Hung[1], W. H. Chuang[1]
[1]TSMC

We present a reliable mega-bit RRAM macro embedded in TSMC 12FFC FinFET logic platform. From extensive learning on 28nm RRAM, we can effectively decrease the endurance failure rate of 12FFC RRAM by optimizing write algorithm based on understanding of RRAM's endurance failure mechanism through 2D Monte-Carlo simulation.

3:35 PM

21-4 Status and Perspectives of Chalcogenide-based Cross-Point Memories (Invited)

Fabio Pellizzer[1], Agostino Pirovano[1], Roberto Bez[1], Russ L. Meyer[1]
[1]Micron Technology

Chalcogenide-based cross-point memories have demonstrated the ability to deliver high performance, cost effective and highly reliable memory technology solutions (e.g. 3DXPoint). Further scaling opportunities have been demonstrated with a Single-chalcogenide Xpoint Memory (SXM) concept that delivers superior performances, a significant cell structure simplification, and a huge scaling potential.

4:25 PM

21-5 Low voltage (<1.8 V) and high endurance (>1M) 1-Selector/1-STT-MRAM with ultra-low (1 ppb) read disturb for high density embedded memory arrays

Elia Ambrosi[1], Cheng-Hsien Wu[1], MingYuan Song[1], Hengyuan Lee[1], Kai-Shin Li[2], Chao-Cheng Lin[2], Chen-Feng Hsu[1], Cheng-Chen Kuo[1], W. N. Chang[2], Y. J. Chen[2], C. H. Lin[2], J. M. Shieh[2], C. H. Shen[2], T. Y. Stanley Lee[1], Tuo-Hung Hou[2], Xinyu Bao[1]
[1]Taiwan Semiconductor Manufacturing Company, [2]Taiwan Semiconductor Research Institute

This work presents a new 1-Selector/1-STT-MRAM (1S1R) device based on SiNGeCTe threshold selector. For the first time, 1e9 read disturb-free cycles are demonstrated in STT-MRAM-based 1S1R. The new device proves low voltage, high speed, low write error rate (<9ppm at 1.7V/ 50ns), along with excellent write endurance (>1M cycles).

4:50 PM

21-6 Enhancing Se-based Selector-only Memory with Ultra-fast Write Speed (~ 10 ns) and Superior Retention Characteristics (> 10 years at RT) via Material Design and UV Treatment Engineering

Jangseop Lee[1], Yoori Seo[1], Sanghyun Ban[1], Dongmin Kim[1], Seongjae Heo[1], Daehwan Kang[1], Hyunsang Hwang[1]
[1]POSTECH

We investigate the effect of material and UV treatment on OTS devices for selector-only memory (SOM) applications. By characterizing OTS with varying material compositions, we identified Se as a key element for SOM operation. The optimized OTS exhibited a large memory window (> 1.2 V) with an ultra-fast write speed (~ 10 ns). Additionally, we demonstrate that interface engineering with UV treatment significantly improved device variability. UV-treated OTS demonstrated excellent retention (> 10 years at RT) and cycling endurance (> 10^8). Analysis of Raman and XPS revealed that SOM properties were determined by the bonding nature associated with the Se.

5:15 PM

21-7 Enhanced Endurance Characteristics in High Performance 16nm Selector Only Memory (SOM)
IL-MOK PARK[1]
[1]SAMSUNG ELECTRONICS

It has been successfully achieved the memory characteristics of a 64Gb array in a single ovonic threshold switch (OTS)-based selector only memory (SOM) with a size of 16nm. We have verified a read window margin (RWM) of 0.5V, effectively operating at speeds below 56ns and with an applied current of 40μA. Particularly, the RWM remains consistently stable even variations in size of the OTS ranging from 15nm to 25nm, providing an advantage for scaling down and offering favorable memory characteristics. However, in SOMs, it remains challenging to maintain the original characteristics of the OTS when external elements penetrate, and the presence of spike current (IS) during turn-on renders the SOM vulnerable in terms of endurance. To address these challenges, we implemented processes aimed at minimizing process-induced damage (PID) to the OTS and optimized the configuration of the cell stack to mitigate the impact of IS. Consequently, we achieved stable write endurance for up to 1E8 cycles and read endurance exceeding 1E9 cycles.

Session 22: Emerging Device and Compute Technology (EDT) - Emerging Devices for AI/Quantum Technologies - Part II
2:15 PM, Continental 5
Co-Chairs: Louis Hutin, CEA-Leti and Veeresh Vidyadhar Deshpande, IIT Bombay

The first four papers in this session cover several implementations of emerging non-volatile memory devices for Compute-in-Memory (CiM) concepts. The last two papers explore a MOSFET-based technological approach to quantum information processing at cryogenic temperatures. Despite energy benefits, NVM-based CiM may be vulnerable to physical access-based attacks. The first paper presents an encryption/decryption technique in FeFET NAND arrays using an XOR-based cipher enabling secure CiM. Reservoir Computing (RC) is well-suited to time-series data processing at the edge. The second paper is an invited presentation of an RC concept based on the switching dynamics of FeFETs, demonstrating high accuracy (>98%) on speech recognition tasks. Physics-inspired algorithms leveraging random device behavior are promising for exploring complex search spaces at a low energy cost. The third paper presents the functional and power consumption analysis for networks of resistively-coupled stochastic Magnetic Tunnel Junctions solving computationally hard optimization problems such as prime factoring. The conductance of emerging NVM devices is a crucial factor in energy-efficient neural accelerators. The fourth paper presents a novel SOT-MRAM device structure with 10ns write speed, leveraging the decoupling of write and read paths and the possibility of resistance tuning to optimize vector-matrix multiplication. Cross-talk management in dense Si spin qubit arrays is of paramount importance to designing scalable systems. The fifth paper presents a novel integration scheme enabling non-invasive charge sensing and suppression of parasitic tunnel coupling in MOS quantum dot arrays for Si spin quantum bits. Classical electronics operating at deep cryogenic temperatures are necessary components of large-scale solid-state quantum computers. The last paper presents I-V characteristics of MOSFETs down to 15mK, along with an in-depth analysis to elucidate the role of band-edge states on the temperature dependence of subthreshold slope and threshold voltage at the lowest temperatures.

2:20 PM
22-1 In-Situ Encrypted NAND FeFET Array for Secure Storage and Compute-in-Memory
Zijian Zhao[1], Yixin Xu[2], James Read[3], Po-Kai Hsu[3], Yixin Qin[1], Tzu-Jung Huang[1], Suhwan Lim[4], Kijoon Kim[4], Kwangsoo Kim[4], Wanki Kim[4], Daewon Ha[4], Thomas Kämpfe[5], Sumitha George[6], Xiao Gong[7], Suman Datta[3], Shimeng Yu[3], Vijaykrishnan Narayanan[2], Kai Ni[1]
[1]Rochester Institute of Technology, [2]Pennsylvania State University, [3]Georgia Institute of Technology, [4]Samsung Electronics Co. Ltd, [5]Fraunhopfer IPMS, [6]North Dakota State University, [7]National University of Singapore

We present a lightweight in-situ encryption/decryption technique for high-density NAND memory. Using ferroelectric FET (FeFET) as a technology platform for demonstration, we show that: i) using a XOR-based cipher, the encryption/decryption can be simply mapped to in-situ array operations; ii) the proposed technique is scalable to multi-level cells (MLC) by encrypting and decrypting bit-by-bit; iii) a unique advantage of applying

XOR-based cipher on NAND array is its capability of supporting high-density and secure compute-in-memory (CiM) with encrypted weights; iv) with integrated NAND FeFET array, we hve successfully demonstrated encryption and decryption operations of single-level cell, MLC, and CiM.

2:45 PM

22-2 Physical Reservoir Computing using HZO-based FeFETs for Edge-AI Applications (Invited)

Shinichi Takagi[1], Kasidit Toprasertpong[1], Eishin Nako[1], Rikuo Suzuki[1], Shin-Yi Min[1], Mitsuru Takenaka[1], Ryosho Nakane[1]
[1]The University of Tokyo

We have proposed and demonstrated reservoir computing (RC) by using HfZrO2/Si FeFETs. We experimentally present the fundamental properties of RC performance and address several methods to enhance RC performance. We experimentally show a classification accuracy of 98.1 % in a speech recognition task.

3:10 PM

22-3 Designing networks of resistively-coupled stochastic Magnetic Tunnel Junctions for energy-based optimum search

Kamal Danouchi[1], Lucile Soumah[1], Corentin Bouchard[2], Florian Disdier[1], Aymen Fassatoui[1], Nhat-Tan Phan[1], Mona Ezzadeen[2], Bertrand Delaet[2], Bernard Viala[2], Guillaume Prenat[1], Lorena Anghel[1], Philippe Talatchian[1], Ioan-lucian Prejbeanu[1], François Andrieu[2], Kevin Garello[1], Louis Hutin[2]
[1]Univ. Grenoble Alpes, CEA, CNRS, Grenoble-INP, SPINTEC, [2]CEA-Leti

After validating a prototyping route, we investigate the impact of CMOS+MTJ building blocks on the quality of stochastic sampling, a key feature in Ising networks. We carry out a functional and power analysis in the frame of Boolean satisfiability solving, showing an 8-bit integer factorization with Simulated Annealing.

3:35 PM

22-4 High RA Dual-MTJ SOT-MRAM devices for High Speed (10ns) Compute-in-Memory Applications

MingYuan Song[1], GuanLong Chen[2], KuanMing Chen[2], Kai-Tai Chang[1], IJung Wang[2], YuChen Hsin[2], Chun-Yi Lin[1], Elia Ambrosi[1], Win-San Khwa[1], Yi-Lun Lu[1], Chen-Yu Hu[1], ShanYi Yang[2], SihHan Li[2], JengHua Wei[2], T. Y. Stanley Lee[1], Allen Y. J. Wang[1], Meng-Fan Marvin Chang[1], Chi-Feng Pai[1], Xinyu Bao[1]
[1]tsmc, [2]ITRI

A novel SOT-MRAM device structure with 1**0**ns write speed and >100x scalable resistance and read current are demonstrated to address the persistent problems of the traditional 2D crossbar array, leveraging its read-write path separation nature.

4:25 PM

22-5 Tunnel and capacitive coupling optimization in FDSOI spin-qubit devices

Benoit Bertrand[1], Biel Martinez[1], Jing Li[1], Bruna Cardoso Paz[2,3], Victor Millory[4], Valentin Labracherie[1], Laurent Brévard[1], Hamza Sahin[1], Grégoire Roussely[1], Aurélien Sarrazin[1], Tristan Meunier[2,3], Maud Vinet[3], Yann-Michel Niquet[4], Boris Brun[4], Romain Maurand[4], Silvano de Franceschi[4], Heimanu Niebojewski[1]
[1]CEA-Leti, [2]CNRS Néel Institute, [3]Siquance, [4]CEA-Irig

We present the ongoing development towards a spin qubit platform compatible with an FDSOI CMOS fabrication flow. We introduce new patterning modules to suppress the diagonal tunnel coupling in QD arrays and fabricate nanowire pairs for non-invasive charge sensing. Numerical simulation provides guidelines for further optimization of the detection sensitivity.

4:50 PM

22-6 Milli-Kelvin Analysis Revealing the Role of Band-edge States in Cryogenic MOSFETs

Hiroshi Oka[1], Hidehiro Asai[1], Takumi Inaba[1], Shunsuke Shitakata[1], Hitoshi Yui[1], Hiroshi Fuketa[1], Shota Iizuka[1], Kimihiko Kato[1], Takashi Nakayama[1], Takahiro Mori[1]
[1]National Institute of Advanced Industrial Science and Technology (AIST)

We revealed the role of band-edge states on MOSFET operation, leveraging the first temperature-dependent SS and V_{th} analysis down to 15 mK. We provided a physical model of I-V behavior over a wide temperature range down to milli-Kelvin, elucidating that the occupancy of immobile band-edge states governs the cryogenic performance.

Session 23: Neuromorphic Computing (NC) - Compute-in-Memory for Deep Learning
2:15 PM, Continental 6
Co-Chairs: Martin Frank, IBM and Duygu Kuzum, University of California San Diego

This session describes advances in compute-in-memory (CiM) technologies and 3D integration for deep learning. Such circuits hold promise for deep learning inference and training by enabling faster and more energy-efficient neural network operations than digital CMOS. The session will be opened with a report on an in-memory compute chip fabricated in 14 nm CMOS technology that employs a carbon-based liner underneath the phase-change material to improve temporal stability and inference accuracy. The second paper reports on low-temperature monolithic 3D integration of carbon nanotube FETs and resistive RAM (ReRAM) arrays to accelerate compute-in-memory for deep neural networks, including a multi-layer perceptron and a ResNet-32. In the following contribution, the ultra-low switching energy of ferroelectric RAM and the reliable read characteristics of ReRAM are leveraged for on-chip inference and learning on the edge. The fourth paper employs custom 3D AND Flash CiM arrays to execute convolution operations in a parallel and highly efficient manner. This is followed by a report on optimized ReRAM devices integrated in 512x512 array tiles, combined with an improved BEOL process and circuits designed to reduce the matrix-vector-multiplications (MVM) error, thereby achieving more accurate deep learning inference. The last paper of this session investigates performance gains for cryogenic compute-in-memory systems through improved device characteristics, with potential applications in cryogenic infrared detectors.

2:20 PM
23-1 In-Memory Compute Chips with Carbon-based Projected Phase-Change Memory Devices
Ghazi Sarwat Syed[1], Kevin Brew[2], Thanos Vasilopoulos[3], Vara Prasad Jonnalagadda[3], Benedikt Kersting[3], Timothy Philip[2], Valeria Bragaglia[3], Esteban Ambrogio Gali[4], Julian Buechel[5], Iason Giannopoulos[3], Manuel Le-Gallo[3], Cheng-wei Cheng[6], Matt BrightSky[6], Vijay Narayanan[7], Nicole Sauliner[2], Abu Sebastian[5]
[1]IBM Research - Europe, [2]IBM Research- Albany, [3]IBM Research- Europe, [4]IBM Research- Almaden, [5]IBM Research--Zurich, [6]IBM Research- Yorktown, [7]IBM Research–T. J. Watson Research Center

Achieving sufficient compute precision in matrix-vector-multiply (MVM) operations is a key challenge for analog in-memory computing (AIMC) that relies on resistive memory devices. A device-level concept that addresses this challenge is that of projected-type phase-change memory (Proj-PCM). Here we present Proj-PCM devices based on carbon-based projection layer (CPL). We integrated these devices onto multi-tile AIMC chips fabricated in 14nm CMOS-technology. CPL is shown to exhibit superior compatibility with the phase-change material layer (PCML) as well as the BEOL process. CPL also provides sufficient tunability of resistance window. The compute tiles with CPL-based Proj-PCM are shown to achieve higher computational precision.

2:45 PM
23-2 3D Stackable CNTFET/RRAM 1T1R Array with CNT CMOS Peripheral Circuits as BEOL Buffer Macro for Monolithic 3D Integration with Analog RRAM-based Computing-In-Memory
Yibei Zhang[1], Yijun Li[1], Jianshi Tang[1], Haitao Xu[2,3], Ran An[1], Qi Qin[1], Zhengwu Liu[1], Lei Gao[2], Ningfei Gao[4], Bin Gao[1], Dong Wu[1], He Qian[1], Huaqiang Wu[1]
[1]Tsinghua University, [2]Beijing Institute of Carbon-based Integrated Circuits, [3]Peking University, [4]Institute of Carbon-based Thin Film Electronics, Peking University

We demonstrated a monolithic 3D integration (M3D) of Si-MOSFET, HfO_x-based analog RRAM and fully functional 3D stackable 1kb one-CNTFET-one-RRAM array. Extensive structural analysis and electrical measurements were carried out. The M3D chip achieving a GPU-equivalent classification accuracy of up to 96.5% in image classification tasks while consuming 39× less energy.

3:10 PM

23-3 Hybrid FeRAM/RRAM Synaptic Circuit Enabling On-Chip Inference and Learning at the Edge

Michele MARTEMUCCI[1,2], François RUMMENS[1], Tifenn HIRTZLIN[2], Simon MARTIN[2], Olivier GUILLE[2], Tarcisius JANUEL[2], Catherine CARABASSE[2], Olivier BILLOINT[2], Julie LAGUERRE[2], Jean COIGNUS[2], Adrien VINCENT[3], Damien QUERLIOZ[4], Laurent GRENOUILLET[2], Sylvain SAÏGHI[3], Elisa VIANELLO[2]
[1]CEA-List, Univ. Grenoble Alpes, [2]CEA-Leti, Univ. Grenoble Alpes, [3]IMS, Univ. Bordeaux, Bordeaux INP, CNRS, [4]Univ. Paris-Saclay, CNRS

This paper presents an experimental demonstration of a hybrid FeRAM/RRAM synaptic circuit. It incorporates Metal-Ferroelectric-Metal stacks, exhibiting native FeRAM behavior and functioning as RRAMs after forming. By leveraging advantages of FeRAMs, e.g., ultra-low switching energy, and the non-disruptive reading of RRAMs, this circuit enables inference and learning at the Edge.

4:00 PM

23-4 First Demonstration of Innovative 3D AND-Type Fully-Parallel Convolution Block with Ultra-High Area-and Energy-Efficiency

Jangsaeng Kim[1], Jiseong Im[1], Jonghyun Ko[1], Soochang Lee[2], Dongseok Kwon[1], Wonjun Shin[1], Joon Hwang[1], Ryun-Han Koo[1], Woo Young Choi[1], Jong-Ho Lee[1,3]
[1]Department of ECE and ISRC, Seoul National University, [2]Memory Division, Samsung Electronics Co., [3]Ministry of Science and ICT

We propose for the first time a novel 3D AND-type flash memory array for a fully-parallel convolution block (FPCB). The FPCB achieves area- and energy-efficient convolution and fully-connected operations. By reducing the number of cells and line resistance, the FPCB reduces ~96% and ~74% of area occupancy and energy consumption.

4:25 PM

23-5 A Holistic methodology Toward Large-scale AI Implementation using Realistic ReRAM based ACiM from Cell to Architecture

Sangsu Park[1], Jihun Kim[1], Wontae Koo[1], Youngjae Kwon[1], Dongik Suh[1], Sangmin Lee[1], Seonghun Lee[1], kayoung Kim[1], Eungu Han[1], Jaeyeon Lee[1], Jongil Kim[1], Kyusung Kim[1], Yeongnam Lim[1], Youngbae Ahn[1], Eunkyung Park[1], Seungwook Ryu[1], Seonghyun Kim[1], Namkyun Park[1], Hoseok Em[1], Seokjoon Kang[1], Junho Cheon[1], Euiseok Kim[1], Jaeyun Yi[1], Kyunhoon Kim[1], Taehoon Kim[1], Seho Lee[1], Myunghee Na[1], Seonyong Cha[1]
[1]SK hynix Inc.

A scalable 256kb 1T1R array-based wafer-level realistic holistic evaluation platform and methodology was demonstrated for the improvement of ReRAM ACiM cell characteristics. Combining cell, PnV, BEOL and circuit improves major metrics, in terms of weight retention by 90%, MAE_{MAC}, by 87%, inference accuracy by 124%.

4:50 PM

23-6 Cool-CIM: Cryogenic Operation of Analog Compute-In-Memory for Improved Power-efficiency

Wei-Chun Wang[1], Rakshith Saligram[1], Sudarshan Sharma[1], Minah Lee[1], Amol Domaji Gaidhane[2], Yu Cao[2], Arijit Raychowdhury[1], Suman Datta[1], Saibal Mukhopadhyay[1]
[1]Georgia Institute of Technology, [2]Arizona State University

Analog computing-in-memory is a promising technology that performs computation on the bitlines to alleviate memory bottleneck, but the power consumption of peripheral circuits limits its power efficiency. This work shows that a cryogenically cooled ACIM (Cool-CIM) can leverage improved device characteristics to lower the operating voltage of peripheral circuits. Circuit simulations with empirically calibrated models of 14nm FinFET

at cryogenic temperature show 54% reduction in EDP and 80% increase in TOPS/W for voltage optimized cryogenic ACIM compared to 300K operation. This study establishes the feasibility of in-sensor processing of analog signals in cryogenic infrared sensors.

Session 24: Modeling and Simulation (MS) - 3D DRAM and Ferroelectric Memories
2:15 PM, Continental 7-9
Co-Chairs: Jiezhi Chen, Shandong University and Giuseppe Iannaccone, University of Pisa

This session includes six excellent papers that describe recent advances in the area of ferroelectric usages in DRAM and non-volatile memories. The first paper, by Dipjyoti Das from Georgia Tech., proposes a novel ferroelectric gate stack for NAND applications with experimental demonstration and modeling. The second paper, by Chen-Yi Cho from National Yang Ming Chiao Tung University, describes a newly developed multi-domain FE wake-up model towards deep insights on the origins of wake-up of ultrathin ferroelectric Hf0.5Zr0.5O2. The third paper, by Zhao-Yi Yan from Tsinghua University propose a compact Liouville model and experimentally verifies its predictive capability in dynamic behaviors of the circuits. The fourth paper, by Deng from Rochester Institute of Technology, addresses the comparative advantages of two-transistor n-capacitor FERAM cells for high-density 3D ferroelectric memories. The fifth paper, by Xu from IMECAS, proposes a variability-aware compact model for independent dual gate FETs based on IGZO for analog computing-in-memory. Finally, the sixth paper by Jiao and Zhou, from National University of Singapore, presents the demonstration and the modeling of an IGZO-base ferroelectric modulated diode with largely enhanced memory window with respect to FEFETs.

2:20 PM
24-1 Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications
Dipjyoti Das[1], Hyeonwoo Park[1], Zekai Wang[1], Chengyang Zhang[1], Prasanna Venkatesan Ravindran[1], Chinsung Park[1], Nashrah Afroze[1], Po-Kai Hsu[1], Mengkun Tian[1], Hang Chen[1], Winston Chern[1], Suhwan Lim[2], Kwangsoo Kim[2], Kijjoon Kim[2], Wanki Kim[2], Daewon Ha[2], Shimeng Yu[1], Suman Datta[1], Asif Islam Khan[1]
[1]Georgia Institute of Technology, [2]Samsung Electronics Co. Ltd

We present a novel dipole engineering scheme for ferroelectric gate stack design, by insertion of an Al_2O_3 layer in the middle of the ferroelectric to enhance the MW. A numerical model of the gate stack was calibrated to the experimental data. A comprehensive design space exploration of the gate stack of FEFETs, based on the model, reveals a pathway to achieving a 12 V MW while satisfying the constraints of vertical NAND flash technology: a total gate stack thickness of 20 nm and a write voltage ≤15 V.

2:45 PM
24-2 Wake-Up of Ultrathin Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$: The Origin and Physical Modeling
Chen-Yi Cho[1], Tzu-Yi Chao[1], Tzu-Yao Lin[1], I-Ting Wang[2], Yu-Sheng Chen[3], Yi-Ching Ong[3], Yu-De Lin[4], Po-Chun Yeh[4], Shyh-Shyuan Sheu[4], Tuo-Hung Hou[1]
[1]National Yang Ming Chiao Tung University, [2]Taiwan Semiconductor Research Institute, [3]Taiwan Semiconductor Manufacturing Company, [4]Industrial Technology Research Institute

A new mechanism, referred to as interfacial-layer soft breakdown (IL-SBD), is proposed to elucidate the wake-up behavior in the ultrathin Hf0.5Zr0.5O2(HZO) capacitor. This model accurately reproduces the trend of thickness-dependent wake-up behavior, emphasizing the utmost significance of IL optimization in ultrathin HZO.

3:10 PM
24-3 A Liouville Model for Polycrystalline Ferroelectrics Emphasizing Kinetic Integrity and Deployability in Circuits with Charge and Current Constraints
Zhao-Yi Yan[1,2], Ruiting Zhao[1,2], Zhenze Wang[1,2], Tian Lu[1,2], Houfang Liu[1,2], Kan-Hao Xue[3], Xiangshui Miao[3], Yi Yang[1,2], Tian-Ling Ren[1,2]
[1]School of Integrated Circuits, Tsinghua University, Beijing, China, [2]Beijing National Research Center for

Information Science and Technology, Tsinghua University, Beijing, China, [3]School of Integrated Circuits, Huazhong University of Science and Technology

Liouville-formula from statistical mechanism is invoked in the Landau-Khalatnikov-Preisach model to give an analytical expression to account for the statistical effect in the polycrystalline ensemble of $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric capacitor, which is considered its further application in circuit-level simulations. The model is extensively validated with measurement data of the fabricated devices.

4:00 PM

24-4 Comparative Advantages of 2T-nC FeRAM in Empowering High Density 3D Ferroelectric Capacitor Memory

Shan Deng[1], Yi Xiao[2], Zijian Zhao[1], Tzu-Jung Huang[1], Thomas Kampfe[3], Vijaykrishnan Narayanan[2], Kai Ni[1]
[1]Rochester Institute of Technology, [2]Pennsylvania State University, [3]Fraunhofer IPMS

We study ferroelectric capacitor memories and demonstrate comparative advantages of 2TnC (Two transistors-n metal-ferroelectric-metal (MFM) capacitors) in scalability, reliability, and feasibility of dense 3D integration and operation. We show that: i) the sensing and scalability issues of conventional FeRAM rooted in its charge-based sensing; ii) FeMFET suffers from the poor reliability and scaling challenges; iii) the 2T-nC can be exploited to address their issues in scalability, density and reliability; iv) through comprehensive experimental and theoretical studies, the design space is explored; v) the integration and operation of 2T-nC FeRAM arrays in 2D and 3D configurations is investigated, demonstrating their potential for improved density and operation.

4:25 PM

24-5 Reliability-Aware Ultra-Scaled IDG-InGaZnO-FET Compact Model to Enable Cross-layer Co-design for Highly Efficient Analog Computing in 2T0C-DRAM

Lihua Xu[1], Kaifei Chen[1,2], Zhi Li[1,2], Jingrui Guo[1,2], Linfang Wang[1,2], Shijie Huang[1,2], Yue Zhao[1,2], Zhidao Zhou[1,2], Chunmeng Dou[1,2], Guanhua Yang[1], Lingfei Wang[1,2], Ling Li[1,2]
[1]State Key Lab of Fabrication Technologies for Integrated Circuits, IMECAS, Beijing, China, [2]University of the Chinese Academy of Sciences, Beijing, China

Ultra-scaled independent-dual-gate (IDG) InGaZnO-FET (~ 26 nm) can potentially lead to highly energy- and area-efficient computing-in-memory (CIM) structures due to its low leakage, extended operational flexibility, and capability for 3D integration. However, its complicated operation principle, increased variation sources, and enlarged parasitic effect hinder device modeling and circuit design. To address these issues, a reliability-aware compact model (RaCM) is developed to describe the surface potential with the IDG coupling effect and excellently agree with fabricated device measurements. Supported by experiments and TCAD calibrated model with variation and degradation, we firstly propose an IDG-2T0C multi-bit computing cell with diode-connected write strategy suppressing variations and independent-gate enhanced data integrity and retention schemes. Furthermore, with RaCM enabled device and circuit co-optimization, a 3D all-in-time-domain (ATD) CIM architecture is proposed. RaCM and 28-nm CMOS hybrid circuit simulation shows it achieves a normalized energy-efficiency (EF) up to 2766 TOPS/W, advancing >3× improvements over previous arts, and a CIFAR-10 inference accuracy loss < 2% after 1000s.

4:50 PM

24-6 First BEOL-compatible IGZO Ferroelectic-Modulated Diode with Drastically Enhanced Memory Window: Experiment, Modeling, and Deep Understanding

Leming Jiao[1], Zuopu Zhou[2], Zijie Zheng[2], Kaizhen Han[2], Qiwen Kong[2], Xiaolin Wang[2], Haiwen Xu[2], Jishen Zhang[2], Chen Sun[3], Yuye Kang[1], Gengchiau Liang[1], Xiao Gong[1]
[1]National University of Singapore, [2]National Univerisity of Singapore, [3]national university of Singapore

Tackling the key challenge of the weak erase in oxide semiconductor FeFETs, for the first time, we experimentally demonstrate a back-end-of-line-compatible IGZO-based ferroelectric-modulated diode, which effectively doubles the memory window of the FeFET fabricated under the same process conditions. To provide a clear understanding of the MW enhancement, we develop and establish a comprehensive simulation

framework that reveals the interplay between ferroelectric polarization and the current rectified by the metal-semiconductor Schottky diode. Furthermore, through a combination of experimental measurement and theoretical calculation, we validate the performance of our novel FMD device in overcoming the weak erase problem of OS FeFETs.

Session 25: Sensors, Mems, and Bioelectronics (SMB) - Thin Film Transistors and Microsensors for Bio/Chemical Detection
2:15 PM, Imperial A
Co-Chairs: Marco Tartagni, University of Bologna and Mina Rais-Zadeh, NASA JPL

This session focuses on novel microsensors and integrated thin film transistors (TFTs) for chemical and biomedical detection. It includes 6 papers that describe recent advances in the areas of thin film transistors and integrated sensing architectures for biology and chemical analysis. The first paper with lead author from Shandong University describes a field programmable large format active matrix for high resolution droplet manipulation. The group led by Westlake University in China presents a TFT active-matrix pH sensor with low operating voltage in the second paper. The third paper from IBM, USA, is an invited presentation on silicon-based reference electrodes for portable in-ground sensors. The proposed electrodes will allow long term measurement in chemically harsh soil medium. The fourth paper is from imec and discusses a nanowell field effect transistor (FET) for molecular detection. It places a 25 nm size nano-well in the center of the silicon fin-FET to detect single stranded DNA molecules with high sensitivity. The fifth paper from Stanford University discusses a device design to mitigate the effect of strain on the performance of carbon nanotube (CNT) based TFTs. The final paper in the session is from imec and illustrates a novel dual-wavelength neural probe using CMOS photonics. The probe is capable of cell-level specific neuro-modulation using optogenetics.

2:20 PM
25-1 Field programmable digital microfluidics chip for high-throughput droplet array manipulation
Jun Yu[1], Shengzhe Jiang[1], Dongping Wang[2], Chunyu Chang[2], Zhiqiang Jia[3], Maohua Du[4], Subao Shi[4], Jiahao Li[5], Wenfei Dong[2], Hanbin Ma[2,4], Arokia Nathan[1,6]
[1]Shandong University, [2]CAS Key Laboratory of Bio-Medical Diagnostics, Suzhou Institute of Biomedical Engineering and Technology, Chinese Academy of Sciences, [3]School of Mechanical and Electrical Engineering, Changchun University of Science and Technology, [4]Guangdong ACXEL Micro & Nano Tech Co., Ltd., [5]ACX Instruments Ltd, [6]Darwin College, Cambridge University

We present a field programmable active-matrix digital microfluidics chip for biological applications, where we demonstrate high-throughput droplet manipulation, as well as single-cell generation. The fabricated microfluidics chip comprises 640×280 pixels that can be independently addressed to execute parallel concurrent droplet generation and single-cell operation.

2:45 PM
25-2 Active-Matrix Potentiometric Sensors with Low Operating Voltage of 0.05 V for High-Resolution Mapping of pH and Cellular Microenvironment
Bowen Zhu[1], Huihui Ren[1], Dingwei Li[1], Min Wang[1], Tingjie Tang[1], Yitong Chen[1], Yan Wang[1], Qi Huang[1], Chengchen Guo[1]
[1]Westlake University

In this work, we develop active-matrix potentiometric sensors that integrate pH sensing and mapping capabilities by utilizing field-effect transistor (FET) sensors based on solution-processed oxide semiconductors. Their high electrical performance enables the successful integration of a 16 × 16 active-matrix FET sensor array for high-resolution pH mapping.

3:10 PM
25-3 Silicon Device-Based Sensing for Sustainability (Invited)
Sufi Zafar[1], Thomas Picunko[1], Cyril Cabral, Jr.[1], Marinus Hopstaken[1], Paul Solomon[1], Hendrik Hamann[1]
[1]IBM TJ Watson Research Center

Sustainable agriculture is mainly limited by the lack of subterranean chemical sensors that measure nutrients near the roots of plants. This study addresses this technology gap. It demonstrates silicon device-based electronic sensors with a novel reference electrode that enables continuous subterranean chemical sensing, essential for more accurate AI-based precision agriculture.

4:00 PM
25-4 Nanowell Field-Effect Transistors for Highly Sensitive Molecular Detection
Lijun Liu[1,2], Sybren Santermans[1], David Barge[1], Jacobus Delport[1], Ashesh Ray Chaudhuri[1], Kherim Willems[1], Seungkyu Ha[1], Simone Severi[1], Pol Van Dorpe[1,2], Koen Martens[1,2]
[1]imec, [2]KU Leuven

We report a novel, highly sensitive bio-molecular sensor device, nanowell FET. A 25nm size nanowell resides in a 35-40nm Si FinFET, which acts as an enhanced molecular sensing region. Near-ideal device performance and doubled our DNA signal to 40mV, which is a major step toward single-molecule sensing with cmos-based FETs.

4:25 PM
25-5 A Device Design Approach to Mitigate Strain Impact on Stretchable Carbon-Nanotube Thin-Film Transistors
Can Wu[1], Donglai Zhong[1], Weichen Wang[1], Yuanwen Jiang[1], Yuya Nishio[1], Yujia Yuan[1], Jeffrey B.-H. Tok[1], Zhenan Bao[1]
[1]Stanford University

Intrinsically stretchable electronics offer mechanical compatibility with various curvilinear objects, opening possibilities for emerging applications inaccessible by conventional rigid or flexible electronics. Recent advancements have led to significant enhancement of stretchable transistor performance (mobility of >10cm^2/V·s at sub-10μm channel length), rivaling that of flexible electronics. However, under strain, intrinsic stretchability introduces inherent large changes in device characteristics, limiting their practical applications. Here we propose a circular transistor design to mitigate strain effect on electrical characteristics, achieving a reduction of strain-induced on-current variation from 56% to 3% by counteracting the performance variations observed across different segments of a 360^o transistor channel.

4:50 PM
25-6 Dual-wavelength neural probe for simultaneous opto-stimulation and recording fabricated in a monolithically integrated CMOS/photonics technology platform
Pieter Neutens[1], John O'Callaghan[1], Jef De Ceulaer[1], Enrico Tonon[1], Marleen Welkenhuysen[1], Carolina Mora Lopez[1], Alexandru Andrei[1], Jan Putzeys[1], Md. Mahmud-Ul-Hasan[1], Hendrikus Tilmans[1], Barundeb Dutta[1]
[1]imec, Kapeldreef 75, Leuven, Belgium

We present a monolithically integrated CMOS and photonics platform. This platform is co-integrated with a 130-nm SOI-based 6-level Al-BEOL. Through this platform, we demonstrate a neural probe that integrates a high-density array of 960 electrodes and 384 recording channels, along with 14 programmable optical emission sites for two visible wavelengths.

Session 26: Power, Microwave/Mm-Wave and Analog Devices/Systems (PMA) - Recent Advances in Wide Bandgap Materials and Devices for Power Electronics
2:15 PM, Imperial B
Co-Chairs: Takuya Maeda, University of Tokyo and Veronique Sousa, CEA-Leti

This session includes 6 papers that describe recent advances of wide bandgap (WBG) materials and devices for power electronics. The first paper, from Peking University, demonstrates 6.5 kV E-mode active-passivation p-GaN gate HEMT on a sapphire substrate with ultralow dynamic Ron. The second paper, from Toyota R&D labs., presents polarization engineering in AlSiO/p-GaN MOSFETs using AlN interlayers formed by PEALD. The

channel mobility over 300 cm2/V•s was achieved. The next paper, from Nagoya Univ., demonstrates AlN-based vertical p-n diodes on an AlN bulk substrate with dopant-free distributed-polarization doping. Clear rectification characteristics with the record breakdown field of 7.3 MV/cm was achieved. The next paper, from Hitachi Ltd., reports the first demonstration of 6.5 kV-class SiC trench-etched double-implantation (TED) IGBTs. The next paper, from Virginia Tech., presents 2 kV & 0.7 mΩ•cm2 vertical p-NiO/n-Ga2O3 super junction SBDs. The final paper, from Waseda Univ., reports diamond p-MOSFETs with oxidized silicon termination. The device achieved the channel mobility over 150 cm2/V•s and |Vth| higher than 3 V, allowing normally-off operation for power IC.

2:20 PM

26-1 6500-V E-mode Active-Passivation p-GaN Gate HEMT with Ultralow Dynamic R_{ON}

Jiawei Cui[1], Jin Wei[1], Maojun Wang[1], Yanlin Wu[1], Junjie Yang[1], Teng Li[1], Jingjing Yu[1], Han Yang[2], Xuelin Yang[2], Jinyan Wang[1], Xiaosen Liu[3], Daisuke Ueda[4], Bo Shen[2]
[1]School of Integrated Circuits, Peking University, Beijing, China., [2]School of Physics, Peking University, Beijing, China., [3]School of Integrated Circuits, Tsinghua University, China., [4]Center of Low-Temperature Plasma Sciences, Nagoya University, Japan

This work demonstrates an E-mode active-passivation p-GaN gate HEMT (AP-HEMT) with breakdown voltage beyond 6500 V and a low R_{ON} of 38.2 Ω·mm ($R_{ON,SP}$ = 33.62 mΩ·cm^2). The AP-HEMT enables the demonstration of ultralow dynamic R_{ON}/static R_{ON} = 1.02 for V_{DS-OFF} = 4500 V.

2:45 PM

26-2 Polarization Engineering in AlSiO/*p*-type GaN MOSFETs Using AlN Interlayers Formed by Plasma-Enhanced Atomic Layer Deposition

Kenji Ito[1], Tetsuo Narita[1], Hiroko Iguchi[1], Shiro Iwasaki[1], Daigo Kikuta[1], Emi Kano[2], Nobuyuki Ikarashi[2], Kazuyoshi Tomita[2], Masahiro Horita[2], Jun Suda[2]
[1]Toyota Central R&D Labs., Inc., [2]Nagoya University

Polarization engineering by AlN interlayers deposited via plasma-enhanced atomic layer deposition was demonstrated in AlSiO/*p*-type GaN MOSFETs. A crystalline AlN interlayer enhanced channel mobility and induced spontaneous polarization charges at the AlN/GaN interface. The threshold voltage was succesfully controlled by both the interlayer thickness and the p-type doping concentration.

3:10 PM

26-3 Demonstration of AlN-based Vertical p-n Diodes with Dopant-Free Distributed-Polarization Doping

Takeru Kumabe[1], Akira Yoshikawa[1,2], Maki Kushimoto[1], Yoshio Honda[1], Manabu Arai[1], Jun Suda[1], Hiroshi Amano[1]
[1]Nagoya University, [2]Asahi Kasei Corporation

Nearly ideal AlN-based vertical p-n diodes are demonstrated utilizing dopant-free distributed-polarization doping (DPD). The fabricated devices exhibited excellent electrical properties, including a desired effective doping concentration, a low turn-on voltage, a low on-resistance, and a high breakdown electric field. These results highlight the DPD's usefulness for high-performance AlN-based power devices.

4:00 PM

26-4 First Demonstration of Trench-shaped 6.5-kV n-channel SiC IGBT with Trench-etched Double-diffused MOS (TED-MOS) Structure

Naoki Watanabe[1], Haruka Shimizu[1], Akio Shima[1]
[1]Hitachi, Ltd.

We experimentally demonstrated the first trench-shaped 6.5-kV SiC IGBT by utilizing the trench-etched double-diffused MOS (TED-MOS) structure. It significantly improved the on-state performance of SiC IGBTs with

proper blocking operation. The TED-MOS SiC IGBT also exhibited smaller switching losses due to a small feedback capacitance and large electron injection.

4:25 PM

26-5 2 kV, 0.7 mΩ•cm^2 Vertical Ga_2O_3 Superjunction Schottky Rectifier with Dynamic Robustness

Yuan Qin[1], Matthew Porter[1], Ming Xiao[1], Zhonghao Du[2], Hongming Zhang[2], Yunwei Ma[1], Joseph Spencer[1,3], Boyan Wang[1], Qihao Song[1], Kohei Sasaki[4], Chia-Hung Lin[4], Ivan Kravchenko[5], Dayrl P Briggs[5], Dale K Hensley[5], Marko Tadjer[3], Han Wang[2], Yuhao Zhang[1]
[1]Virginia Polytechnic Institute and State University, [2]University of Southern California, [3]U.S. Naval Research Laboratory, [4]Novel Crystal Technology, [5]Oak Ridge National Laboratory

We report the first demonstration of a vertical superjunction device in ultra-wide bandgap Ga_2O_3. Ga_2O_3 superjunction Schottky diodes show a on-resistance of 0.7 mΩ·cm^2 and breakdown voltage of 2000 V, the trade-off of which are among the best in all power Schottky diodes. High-temperature and switching robustness are also demonstrated.

4:50 PM

26-6 Oxidized Silicon Terminated Diamond p-MOSFETs with Channel Mobility >150 cm^{2}V^{-1}s^{-1} and $|V_{TH}|$> 3V Normally-off for Complementary Power Circuits

Hiroshi Kawarada[1,2], Kousuke Ota[1], Yu Fu[1], Kento Narita[1], Xiahua Zhu[1], Atsushi Hiraiwa[1], Tetsuya Fujishima[2]
[1]Waseda University, [2]Power Diamond Systems, Inc.

Oxidized silicon terminated (C-Si-O) diamond surface has been applied for lateral and vertical MOSFETs. C-Si-O bonds instead of C-O-Si bonds are key to fabricate higher channel mobility of diamond p channel MOSFETs (p-MOSFETs). The hole channel mobility exceeds 150 cm^{2}V^{-1}s^{-1} which is higher than the electron mobility of SiC n-MOSFETs. The threshold voltage V_{TH} of diamond p-MOSFET is negatively large enough (V_{TH} < -3V) for normally-off operation at high voltage circuits. Maximum drain current densities $I_{D,Max}$ were >300 mAmm^{-1} in lateral FETs and >200 mAmm^{-1} in vertical FETs. They are the highest in normally-off operation of diamond p-FETs.

Session 27: - Evening Panel: AI: Semiconductor Catalyst? Or Disrupter?
8:00 PM, Continental 4-5
Moderators G. Dan Hutcheson, TechInsights
Co-Organizer: John Chen, NVIDEA

Artificial Intelligence has long been a hot topic. In 2023 it became super-heated when large language models became readily available to the public. This year's IEDM will not be a rehashing of what's been dragged through media. Instead, it will bring together industry experts to have a conversation about how AI is changing the semiconductor industry and to ask them how they are using AI to transform their efforts. The topics will be wide ranging from how AI will drive demand for semiconductors, to how it's changing design and manufacturing, and even to how it will change the jobs and careers of those working in it.

Panelists:
Stelios Diamantidis, Synopsys
Ira Leventhal, Advantest
Chris Horng-Dar Lin, TSMC
Nicole Saulnier, IBM
Anantha Sethuraman, Applied Materials

Wednesday, Dec. 13
Session 28: Focus Session 1: - PMA/MS - Focus Session - Sustainability in Semiconductor Device Technology and Manufacturing

9:00 AM, Grand Ballroom A
Co-Chairs: Brianna Klein, Sandia National Labs and Vita Pi-Ho Hu, National Taiwan University

This is a focus session on sustainability in semiconductor device technology and manufacturing which aims to reduce carbon emission. First, IMEC shows a life cycle analysis of CMOS technologies from N28 to A14 based on the high-volume IC fabrication tools. The approach provides sensitivity analysis and highlights high-impact processes that could be improved to reduce environmental footprints in pathfinding technologies. The next paper, presented by Applied Materials, developed new tools for monitoring and modeling the systems' energy use and emissions impact that incorporate principles and practices aligned with industry standards. These tools have enabled engineering teams to include principles of sustainability into the design of new products with quantifiable results. The third paper is by ASML and discusses the management of their EUV photolithography systems including cooling system, hydrogen re-use, sleep mode, and material recycling. Next, Samsung discusses the development of the technology for prediction of turbulent flow and the diffusion of airborne molecular contaminants (AMC) inside of fabrication facilities. Their work also includes the reduction of AMC and emissions, and the CO2 capture and utilization to operate fabs with low energy and high efficiency, improve yields, and reduce air pollution. The fifth paper will be presented by TechInsights, which investigated Greenhouse Gases (GHGs) emissions in the semiconductor industry and developed a commercial model of leading edge 300mm fabs. STMicroelectronics is the sixth paper, and they have developed the Sustainable Technology program based on a robust life cycle approach, capturing social and environmental footprint at every stage of the product's life.

9:05 AM
28-1 Cradle-to-gate Life Cycle Assessment of CMOS Logic Technologies (Invited)
Lizzie Boakes[1], Marie Garcia Bardon[1], Vincent Schellekens[1], Cedric Rolin[1], I-Yun Liu[1], Benjamin Vanhouche[1], Gioele Mirabelli[1], Farid Sebaai[1], Laurent Van Winckel[1], Emily Gallagher[1], Lars-Ake Ragnarsson[1]
[1]Imec

This paper presents a life cycle analysis of logic technology nodes N28 to A14 based on bottom-up modeling of a high-volume IC fabrication plant. This holistic approach provides granular results, enables sensitivity analysis, and highlights high-impact processes that could be improved to reduce environmental footprints in existing and pathfinding technologies.

9:30 AM
28-2 Sustainability-Aware Technology Development at Applied Materials (Invited)
Benjamin Jay Gross[1], E. Neville Reyes[1], S. Kapadia[1]
[1]Applied Materials

We have developed new tools for monitoring and modeling our systems' energy use and emissions impact that incorporate principles and practices aligned with industry standards. These tools have enabled our engineering teams to include principles of sustainability into the design of our new products with quantifiable results.
9:55 AM
28-3 EUV energy efficiency (Invited)
Theo Thijssen[1], Ton van der Net[1], Toni Janssen[1], Carlo Luijten[1]
[1]ASML Netherlands B.V.

Energy efficiency of the ASML EUV lithography systems is being improved by increasing productivity while at the same time reducing absolute energy consumption. The latter is achieved via sleep mode, hydrogen re-use and tower-cooled process cooling water.

10:45 AM
28-4 Sustainable Environmental Technologies for Advanced Semiconductor Manufacturing Intelligent FAB (Invited)
Hyun Chul Lee[1], Sehyeong Oh[1], Dong Sik Yang[1], Min Seok Koo[1], Dong Jin Ham[1], Joonseon Jeong[1], Sungwoo Kang[1], Jaehee Chang[1], Hyeon-su Heo[1], Mijong Kim[1], Jonghyun Ha[1], Su Keun Kuk[1], Dong Jin Lee[1], Jai Young

Chung[1], Dongwook Kim[1], Jaeeun Kim[1], Jong-Min Lee[1], Hyuk Jae Kwon[1], Jinkyu Kang[1], Jae-Young Kim[1], Yu Kyung Jung[1], Wooyong Shim[1], Seung Hoon Song[1], Jinha Kim[1], Jaesoo Lee[2], Dohoon Kim[2], Junghun Nam[2], Da-Hee Lee[2], Hojun Choi[2], Se-Yeon Kim[2], Min-Soo Suh[2], Sangyoon Shin[2], JinHo Kim[2], Yanfang Chen[3], Hwajin Kim[3]
[1]Air Science Research Center, Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd, [2]Global Manufacturing&Infra Technology, Samsung Electronics Co., Ltd, [3]Department of Environmental Health Sciences, Graduate School of Public Health, Seoul National University

We are focusing on providing a sustainable intelligent FAB environment. Thus, it may be essential to accurately predict and remove airborne molecular contaminants (AMC) which cause defects during manufacturing process. Also, the study for secondary aerosol formation inside and outside of FAB will give insights for sustainable intelligent FAB environment.

11:10 AM
28-5 Modeling 300mm Wafer Fab Carbon Emissions (Invited)
Scotten W Jones[1]
[1]TechInsights

A carbon emissions model for 300mm wafer fabs is described. The basics of the model calculations and examples of the model outputs are presented. Key challenges to reducing emissions, now, and in the future, are identified.

11:35 AM
28-6 Developing Sustainable Technologies for a more Sustainable Future (Invited)
Serge Nicoleau[1], Jean-Louis Champseix[1], Dominique Tagarian[1], Frederic Boeuf[1], Philippe Quinio[1]
[1]STMicroelectronics

In this paper, we present how STMicroelectronics is developing technologies that are key enablers for creating a more sustainable future. These technologies enable our customers to develop responsible applications for safer, greener, and smarter living.

Session 29: Advanced Logic Technology (ALT) - 3D Stacked Transistors
9:00 AM, Grand Ballroom B
Co-Chairs: Lars Liebmann, Intel and Tenko Yamashita, IBM

As lateral scaling, for several decades the primary enabler of VLSI, is becoming increasingly challenging, the semiconductor industry is exploiting dense 3d stacking as an additional path forward. Unlike packaging-based 3d stacking, in which complete chips (or chiplets) are bonded, ‘dense 3d stacking’ extends integration-based scaling by stacking individual transistors. Complementary field effect transistors (CFETs) stack opposite polarity gate-all-around (GAA) or other transistors vertically to eliminate n-to-p spacing from the cell footprint. While promising substantial transistor density improvement, CFETs come with a substantial increase in process and integration complexity. Alternatively, multiple layers of CMOS circuitry can be sequentially integrated and connected at pitches not achievable in hybrid bonding. This session, containing six papers from industry leaders as well as academia, reviews both monolithic and sequential transistor stacking approaches and addresses integration of CFETs with advanced middle of line (MOL), back side power delivery networks (BSPDN), and heterogeneous transistor optimization.

9:05 AM
29-1 3D Stacked Devices and MOL Innovations for Post-Nanosheet CMOS Scaling (Invited)
Naoto Horiguchi[1], Hans Mertens[1], Thomas Chiarella[1], Steven Demuynck[1], Anne Vandooren[2], Anabela Veloso[3], Marie Garcia Bardon[3], Anshul Gupta[1], Giuliano Sisto[3], Victor Vega-Gonzalez[1], Zsolt Tokei[1], Serge Biesemans[1], Julien Ryckaert[3]
[1]imec, [2]imec, Leuven, Belgium, [3]Imec

3D stacked devices without area penalty from device-device space, such as complementary FET (CFET), is promising for post-nanosheet CMOS scaling. New MOL architectures, such as backside power delivery network (BSPDN) or Vertical-Horizontal-Vertical routing style, are required to connect 3D stacked devices without wiring congestions and resistance increase.

9:30 AM

29-2 Demonstration of a Stacked CMOS Inverter at 60nm Gate Pitch with Power Via and Direct Backside Device Contacts

Marko Radosavljevic[1], Cheng-ying Huang[1], Rohit Galatage[1], Munzarin F Qayyum[1], Jami A Wiedemer[1], Evan Clinton[1], David Bennett[1], Hojoon Ryu[1], Nicole K Thomas[1], Patrick Morrow[1], Thoe Michaelos[1], Rambert Nahm[1], Natalie Briggs[1], Anandi Roy[1], Charles C Kuo[1], Sarah Atanasov[1], Susmita Ghose[1], Niels Zussblatt[1], Nitesh Kumar[1], Dincer Unluer[1], Madeleine Beasley[1], Jeffrey Miles Tan[1], Li Huey Tan[1], Matthew Elkins[1], Seda Cekli[1], Richard Hermann[1], Leah Shoer[1], Makram Abd El Qader[1], Umang Desai[1], Trenton Edwards[1], Priyaa Prasad[1], Jeff L Armstrong[1], Mithun Ghosh[1], Yean-An Liao[1], Vadym Kapinus[1], Dhairya Dixit[1], Michael K Harper[1], Phuong Tran[1], Kai Loon Cheong[1], Adnan Fatehi[1], Adedapo A Oni[1], Noel Franco[1], Brian J Krist[1], Matthew V Metz[1], Gilbert Dewey[1], Richard Schenker[1], Mauro J Kobrinsky[1]
[1]Intel Corporation

A device architecture with n-MOS and p-MOS transistors stacked on top of each other is considered a key option to continue scaling in the semiconductor industry. We report experimental demonstrations of scaled devices consist of 3 n-MOS on top of 3 p-MOS nanoribbons with 30nm vertical separation, vertically stacked dual-source/drain epitaxy and dual metal workfunction gate stacks. Moreover, we demonstrate a vertical nanoribbon depopulation process. Finally, by combining 3D stacked CMOS devices with backside power via and direct backside device contacts (BSCON), we demonstrate for the first time fully functional scaled inverters down to contacted poly pitch (CPP) of 60nm.

9:55 AM

29-3 3D sequential integration with Si CMOS stacked on 28nm industrial FDSOI with Cu-ULK iBEOL featuring RO and HDR pixel

Tadeu Mota Frutuoso[1], Valerie Lapras[1], Laurent Brunet[1], Leo Basset[1], Jose Lugo[1], Claire Fenouillet-Beranger[1], Maud Vinet[1], Francois Boulard[1], Yorrick Exbraya[1], Delphine Boutry[1], Olivier Billoint[1], Daphnee Bosch[1], Yves Maneglia[1], Arnaud Peizerat[1], Sylvain Dumas[1], Gilles Sicard[1], Sebastien Kerdiles[1], Joel Kanyandekwe[1], Petros Sideris[1], Vincent Mazzocchi[1], Aurelien Sarrazin[1], Virginie Loup[1], Gaelle Mauguen[1], Christophe Morales[1], Pablo Acosta Alba[1], Viorel Balan[1], Cedric Perrot[1], Julian Sturm[1], C. Euvrard[1], Francois Aussenac[1], A. Janaud[1], J-D Chapon[2], Marc Guillermet[1], S. Guglieri[2], F. Bailly[2], P. Toresani[2], Frank Fournel[1], Mehdi Mouhdach[1], A. Berthoud[1], L-L. Chapelon[2], Mickael Ribotta[1], Fabienne Ponthenier[1], Alexandre Magalhaes[1], Jean Michailos[2], Franck Arnaud[2], Andreia Cathelin[2], Julien Arcamone[1], Didier Lattard[1], Xavier Garros[1], François Andrieu[1], Fred Gaillard[1], Perrine Batude[1]
[1]CEA-Leti, Univ. Grenoble Alpes, France, [2]STMicroelectronics, Crolles, France

This work demonstrates for the first time the 3D sequential integration of CMOS over CMOS with advanced metal line levels (28nm Cu + ULK). A bevel contamination wrap module allows the return of the wafer to Front End Of Line (FEOL) environment required for achieving high performance top FET Si CMOS processing. Additionally, the doped poly-Si ground plane introduced enables top FET dynamic back-biasing and effective DC and HF isolation with underlying metal lines. Finally, this 3DSI platform demonstrates functional 3D ring oscillators as well as a pixel with a 3D single exposure flicker-free High Dynamic Range capability.

10:45 AM

29-4 First demonstration of 3-dimensional stacked FET with top/bottom source-drain isolation and stacked n/p metal gate

Jaehyun Park[1], Wukang Kim[1], Sungil Park[1], Jinchan Yun[1], Kyuman Hwang[1], Jinwook Yang[1], Dahye Kim[1], Jae Won Jeong[1], Chuljin Yun[1], Jinho Bae[1], Jejune Park[1], Sam Park[1], Woong Huh[1], Daihong Huh[1], Suk Yang[1], Junghan Lee[1], Jaehoon Seo[1], Ajeong Kim[1], Kyungseok Oh[1], Donggon Yoo[1], Bong Jin Kuh[1], Daewon Ha[1], Yu

Gyun Shin[1], Jaihyuk Song[1]
[1]Samsung Electronics

We report world's first demonstration of n- and pMOSFET in 3-Dimensional Stacked FET (3DSFET) with vertically stacked n/p metal gate and isolated source/drain between top and bottom FETs.

11:10 AM
29-5 First Demonstration of Monolithic Self-aligned Heterogeneous Nanosheet Channel Complementary FETs with Matched V_T by Band Alignments of Individual Channels
Chien-Te Tu[1], Wan-Hsuan Hsieh[1], Yu-Rui Chen[1], Bo-Wei Huang[1], Yu-Tsung Liao[1], Wei-Jen Chen[1], Yi-Chun Liu[1], Chun-Yi Cheng[1], Hung-Chun Chou[1], Hao-Yi Lu[1], Cheng-Hsien Hsin[1], Geng-Min He[1], Dong Soo Woo[1], Shee-Jier Chueh[1], C. W. Liu[1]
[1]National Taiwan University

Monolithic 3D stacked $Ge_{0.9}Sn_{0.1}$ nanosheet and $Ge_{0.75}Si_{0.25}$ nanosheet complementary FETs with multiple P/N junction isolation by in-situ doped CVD epitaxy are experimentally demonstrated. Heterogeneous channels with common single work function metal gate structure are fabricated as a CMOS inverter with the matched V_T and good voltage transfer characteristics.

11:35 AM
29-6 Complementary Field-Effect Transistor (CFET) Demonstration at 48nm Gate Pitch for Future Logic Technology Scaling
Szuya Sandy Liao[1], Lu Yang[1], Tsung-Kai Chiu[1], Wei-Xiang You[1], Ting-Yun Wu[1], Ku-Feng Yang[1], Wei-Yen Woon[1], Wei-De David Ho[1], Zhi-Chang Lin[1], Hsin Yang Hung[1], Jui-Chien Ray Huang[1], Shao-Tse Huang[1], Min-Chang Tsai[1], Chien-Lin Derick Yu[1], Szu-Hua Chen[1], Kuan-Kan Hu[1], Che Chi Shih[1], Yung-Ta Chen[1], Chun-Yu Liu[1], Han-Yu Lin[1], Cheng-Ting Chung[1], Lilin Su[1], Chi-Yu Jack Chou[1], Yu-Tien Shen[1], Chia-Min Chang[1], Yi-Tan Lin[1], Meng-Yu Lin[1], Wei-Cheng Lin[1], Bing-Hung Richard Chen[1], Chin-Shan Hou[1], Fred Lai[1], Xiaomeng Chen[1], Jeff Wu[1], Chung-Kai Lin[1], Yi-Kan Cheng[1], Hua-Tai Lin[1], Yao-Chin Ku[1], S.S. Lin[1], Li-Chung Lu[1], S.M. Simon Jang[1], Min Cao[1]
[1]Taiwan Semiconductor Manufacturing Company (TSMC)

Abstract— This study establishes the groundwork for an industry-applicable, integrated nanosheet-based monolithic CFET process architecture with a gate pitch of 48nm. By introducing the middle dielectric insolation, inner spacer, and n/p source-drain isolation, the vertically stacked nFET-on-pFET nanosheet transistors yield a survival rate of over 90% and demonstrate high on-state current with low leakage, achieving a healthy six-order of magnitude on/off current ratio. This work sets the stage for further CFET development and paves the way for a practical process architecture that can fuel future logic technology scaling and PPAC advancement.

Session 30: Modeling and Simulation (MS) - Modeling and characterization for DTCO
9:00 AM, Continental 1-3
Co-Chairs: Jing Wang, NVIDIA and Andries Scholten, NXP

This session includes four papers, focusing on various aspects of design-technology co-optimization (DTCO). The session starts with a contribution from Cai (Sun Yat-sen University) on electromigration in backside power delivery networks, which are envisioned for the 2nm node and beyond. The next paper, by Prasad from AMD (invited) stresses the importance of thermal modeling in DCTO for future technologies. The third paper, by Han from the National University of Singapore, presents a new, universal, method to extract contact resistances from experimental data, using dedicated test structures. The session ends with a paper by Davoody (Intel), that uses machine-learning-based algorithms to extract realistic model parameter distributions, accurately describing measured device variability.

9:05 AM
30-1 Electromigration of Backside Power Delivery Networks for PPA-Reliability Tradeoffs at N2 Node

Linlin Cai[1], Yutao Chen[1], Haoyu Zhang[1], Jianwen Lin[1], Binyu Yin[1], Wangyong Chen[1]
[1]Sun Yat-sen University

EM reliabilities of BSPDNs using techniques of BPR, TSVM and BSC are comprehensively investigated by proposed electro-thermal-stress fully coupled simulation method. By studying TTF of different BSPDNs and alternative metal materials, valuable insights are gained to mitigate failure risks and enhance EM reliability for PPA-Reliability tradeoffs at N2 node.

9:30 AM
30-2 Paradigm Shift in Semiconductor Technology Scaling Calling for Advancements in Design Modelling (Invited)
Divya Prasad[1], Girish Kini[1], Sriram Chandrasekaran[1], Sudhanva Gurumurthi[1], Amy Novak[1], Tom Burd[1]
[1]AMD

Semiconductor manufacturing inventions like back-side power, and 3D stacking at the packaging level have driven continued technology scaling despite the slowdown in dimension scaling. While these inventions show promise for enhancing performance, they have elevated the need for thermal and reliability management to be classified as first-class design issues.

9:55 AM
30-3 A Novel Universal Model for Extracting Specific Contact Resistivity with High Resolution, Strong Variation Immunity, and Simple Fabrication Process
Kaizhen Han[1], Yuye Kang[1], Yue Chen[1], Xiao Gong[1]
[1]National University of Singapore

A novel and universal model for extracting specific contact resistivity (ρ_C) named Nano bridge transmission line method (Nano-BTLM) has been proposed with its effectiveness and accuracy comprehensively validated by both TCAD Sentaurus simulations and experiments. The Nano-BLTM offers several advantages, including the elimination of parasitic resistance (R_p), simple fabrication process, highly accurate ρ_C extraction, strong variation immunity, and universal applicability. It fulfils all the essential requirements for characterizing the state-of-the-art advanced metal/semiconductor contacts. To demonstrate the capabilities of Nano-BTLM, extensive investigations have been carried out using metal/ITO contacts as the test vehicle. The studies encompassed the examination of various contact metals and the impact of annealing.

10:20 AM
30-4 Deep Generative Model for Device Variation Modeling
Amirhossein Davoody[1], Ananda S. Roy[1], Sivakumar P Mudanai[1]
[1]Intel Corporation

This study shows for the first time the use of deep generative models to accurately model device variation, addressing the challenge of capturing tail distribution and correlations. Previous research highlights the significance of capturing fine structures in joint parameter distributions for representing electrical measurement distributions.

Session 31: Memory Technology (MT) - MRAM and 2T0C DRAM
9:00 AM, Continental 4
Co-Chairs: Zhiqiang Wei, Avalanche and Shosuke Fujii, Kioxia

This session covers "MRAM and 2T0C DRAM" . It consists of seven papers including five on MRAM and two on 2T0C DRAM technology. First paper from Kioxia shows a novel 14nm MTJ design, offering both high-retention and high speed writing of 5ns. Second paper from TSMC discusses the significance of high-speed embedded memory for future high performance computing (HPC) chips for AI application. Third paper presents the advantages of muti-bit SOT-MRAM utilizing VMCA for Last Level Cache. The fourth paper demonstrates Top-pSOT-MRAM structure, integrated with standard STT-MTJ device, simplifies SOT technology implementation.

Avalanche technology has developed an 8Gb STT-MRAM with superior radiation tolerance, offering a high-density, reliable memory solution for next-generation space computing. Next, the Chinese Academy of Sciences successfully realized a vertically stacked 4F2 2T0C DRAM using channel-all-around IGZO FETs. The last presentation shows a novel dual-gate IGZO DRAM, achieving multi-bit storage without adding complexity.

9:05 AM

31-1 14nm High-Performance MTJ with Accelerated STT-Switching and High-Retention Doped Co-Pt Alloy Storage Layer for 1Znm MRAM

Masahiko Nakayama[1], Soichi Oikawa[1], Chikayoshi Kamata[1], Masaru Toko[1], Shogo Itai[1], Rina Takashima[1], Hideyuki Sugiyama[1], Kenji Fukuda[1], Takeo Koike[1], Masumi Saitoh[1], Junichi Ito[1], Katsuhiko Koi[1]
[1]KIOXIA Corporation

We introduce a new Accelerated STT-switching and High-Retention MTJ using doped Co-Pt alloy MTJ (AccelHR-MTJ). High-retention of >10 years at 90℃ and 5ns high-speed writing were demonstrated in our 14nm AccelHR-MTJ based on the design concept established by micromagnetic simulations. This MTJ technology enables high-density 1Znm STT-MRAM toward SCM applications.

9:30 AM

31-2 High-Speed Embedded Memory for AI and High-Performance Compute

Yih Wang[1]
[1]TSMC

High-speed embedded memory is essential to enable compute efficiency for next generation HPC chip. This paper overviews DTCO innovations in SRAM, digital compute-in-memory architectures, and high-density embedded memory to address performance, energy efficiency and density needs for future AI and HPC computing chips.

9:55 AM

31-3 Ultimate MRAM Scaling: Design Exploration of High-Density, High-Performance and Energy-Efficient VGSOT for Last Level Cache

Mohit Gupta[1], Yang Xiang[1], Fernando Garcia-Redondo[1], Kaiming Cai[1], Dawit Abdi[1], Hsiao-Hsuan Liu[1,2], Siddharth Rao[1], Gaspard Hiblot[1], Sebastien Couet[1], Marie Garcia-Bardon[1], Geert Hellings[1]
[1]imec, [2]KU Leuven

The Voltage-Gated Spin-Orbit-Torque is a unique MRAM that enables multi-pillar SOT through voltage-controlled magnetic anisotropy. In this paper, we explore the scaling potential of multi-pillar VGSOT for last-level cache towards A14 node in terms of macro-level power-performance-area, and profile the required device design space based on a hardware-validated compact model.

10:20 AM

31-4 First BEOL-compatible, 10 ns-fast, and Durable 55 nm Top-pSOT-MRAM with High TMR (>130%)

Kai-Shin Li[1,1], Jia-Min Shieh[1], Yi-Ju Chen[1], Cho-Lun Hsu[1], Chang-Hong Shen[1], Tuo-Hung Hou[1], Chai-Ping Lin[2], Chih-Huang Lai[2], Denny D. Tang[3], Jack Yuan-Chen Sun[4]
[1]Taiwan Semiconductor Research Institute, [2]Department of Materials Science and Engineering, National Tsing Hua University, [3]Industrial Technology Research Institute, [4]International College of Semiconductor Technology, National Yang Ming Chiao Tung University

We demonstrated an advanced Top-pSOT-MRAM structure by fabricating the SOT channel electrode on top of a typical STT-MTJ. A Ru metal layer with high etch selectivity is utilized as the etch-stop layer, enabling the connection between the free layer of the MTJ and the Top SOT channel. Therefore, this Top-pSOT-MRAM device, compatible with STT-MRAM, remarkably exhibits a very high TMR of >130%. It thus intrinsically gives 400°C thermal robustness. The field-free SOT switching as fast as <10 ns with STT assisting is obtained with high endurance (10^{10} cycles). From R-V_{SOT} curve, the switching current density can be reduced to 74 MA/cm^2 by increased STT voltage. This Top-pSOT-MRAM device could be scaled to ~55 nm with the thermal

stability factor (Δ) of 62, targeting for one-month retention time with 1ppm error rate. Our demonstrated BEOL-compatible pSOT devices with high endurance, and high retention can provide a new SOT-MRAM technology for computing-in-memory (CIM) applications.

11:10 AM

31-5 Dual QSPI 8Gb STT-MRAM For Space Applications

Zihui Wang[1], Zhiqiang Wei[1], Guanzhong Wu[1], Longqian Hu[1], Mengchun Wu[1], Uday Chandrasekhar[1], Thin Tran[1], Mourad Baraji[1], Jun Li[1], Ebi Abedifard[1], Yiming Huai[1]
[1]Avalanche Technology

As the demand for advanced memory solutions in space escalates, conventional charge-based memory falls short due to its vulnerability to high-energy particles. The presented STT-MRAM with 8Gb density shows superior radiation tolerance with >125°C 10 years data retention and >10^{14} write endurance, demonstrating unrivaled performance capability for applications in space.

11:35 AM

31-6 First Demonstration of Stacked 2T0C-DRAM Bit-Cell Constructed by Two-Layers of Vertical Channel-All-Around IGZO FETs Realizing 4F2 Area Cost

Chuanke Chen[1], Di Geng[2], Ling Li[1]
[1]Institute of Microelectronics of the Chinese Academy of Sciences, [2]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China

For the first time, we have realized the vertical-stacked 4F2 2T0C DRAM cell constructed by two-layers of Channel-All-Around (CAA) IGZO FETs. The devices fabrication process is BEOL-compatible with the process temperature ≤250℃. The influences of monolithic stack on 1st layer of devices have been investigated. By optimizing the IGZO-ALD deposition process, 2T0C bit-cell constructed by two CAA IGZO FETs is obtained, and a retention time of 75s has been experimentally verified, as well as good reliability. Our results demonstrate the feasibility of 4F2 2T0C bit-cell based on stacked CAA IGZO FETs for high-density 3D DRAM application.

12:00 PM

31-7 Improved Multi-bit Statistics of Novel Dual-gate IGZO 2T0C DRAM with In-cell V_{TH} Compensation and &[Delta]V_{SN}/&[Delta]V_{DATA} Boosting Technique

Kaifei Chen[1], Zhengyong Zhu[2] Wendong Lu[1], Menggan Liu[1], Fuxi Liao[1], Zijing Wu[1], Jiebin Niu[1], Bok-Moon Kang[1], Wang Dan[2], Xie-Shuai Wu[2], Ming-Xu Liu[2], Yong Yu[2], Nan Yang[2], Gui-Lei Wang[2], Kan-Yu Cao[3], Lingfei Wang[1], Di Geng[1], Nianduan Lu[1], Guanhua Yang[1], Chao Zhao[2], Arokia Nathan[4], Ling Li[1] and Ming Liu[1]
[1]Institute of Microelectronics, Chinese Academy of Sciences, [2]Bejing Superstring Academy of Memory Technology, [3]ChangXin Memory Technologies, Inc., [4]Darwin College, Cambridge University

For the first time, one novel dual-gate IGZO DRAM is proposed and demonstrated for multi-bit storage. By this design, 3-bit storage among 25 cells exhibits improved statistical distribution with one order reduction of standard deviation. This work paves the forward way for multi-bit IGZO 2T0C DRAM applications.

Session 32: Reliability Of Systems and Devices (RSD) - FEOL and Memory Reliability

9:00 AM, Continental 5

Co-Chairs: Francesco Puglisi, University of Modena and Reggio Emilia and KyoungChul Jang, SK Hynix

This session focuses on the reliability aspects of front-end-of-the-line and memory devices (e.g., FinFETs, FD-SOI MOSFETs, RRAMs, DRAMs, FeRAMs) related to phenomena associated with dielectric structure and stability, charge trapping and defect generation (e.g., noise, fluctuations, breakdown, phase formation). The session opens with a contributed paper on trap-induced mobility fluctuations in FD-SOI MOSFETs in which the authors propose a methodology to extract both CNF and CMF variability contributions, without analyzing each measurement separately, that can be used also in circuit simulations. The session proceeds with a paper on

flicker noise characterization and modeling in advanced FinFETs: the authors propose a new physical-based model for flicker noise that accounts for multiple noise sources and that can be used to extract the relative contribution of each source from measurements. The third paper proposes an in-depth analysis of TDDB in on- and off-state conditions from DC to high frequency. Results highlight how AC, high-frequency, and low duty cycle waveforms inhibit the IL percolation path formation, which in turn delays the field redistribution that triggers high K degradation, prolonging the device lifetime. Then, an invited paper covers the details of dielectric breakdown in RRAMs and gate stacks, in which hydrogen plasma post-deposition steps are demonstrated to unlock a reverse area scaling trend by which the forming voltage increases at increasing area, beneficial for technology integration. The trend is replicated by a newly proposed statistical modeling approach. The session continues with a paper on the end-to-end reliability characterization of DDR5 DRAMs in which an effective methodology for predicting the intrinsic failure rates <0.01ppm using hundreds of DRAM chips in one wafer is proposed. The session closes with a paper that presents a reliability-robust 256 kbit FeRAM chip with wake-up free, optimized performance, achieved by means of pre-annealing engineering and ozone treatment that promote tensile stress and suppress tetragonal phase formation.

9:05 AM

32-1 Variability of Trap-induced Mobility Fluctuations in Nanoscale Bulk and FD-SOI MOSFETs

Owen Gauthier[1,2], Sebastien Haendler[1], Quentin Rafhay[3], Christoforos Theodorou[4]
[1]ST Microelectronics, [2]IMEP-LAHC, [3]Grenoble INP / IMEP-LAHC, [4]CNRS / IMEP-LAHC

Low frequency noise (LFN) and random telegraph noise (RTN) are statistically analyzed for 40 nm Bulk and 28 nm FD-SOI MOSFETs. A new model is proposed to directly extract the variability contributions of both carrier number fluctuations (CNF) and correlated mobility fluctuations (CMF), without needing to analyze each measurement separately.

9:30 AM

32-2 Comprehensive Understanding of Flicker Noise in Advanced FinFET Technology: from Noise Sources Separation to Physical-based Modeling

Junjie Wu[1], Pengpeng Ren[1], Chenyang Zhang[1], Yu Xiao[1], Yongkang Xue[1], Yu Li[2], Xiaolin Wang[1], Lining Zhang[2], Junhua Liu[3], Jianfu Zhang[4], Runsheng wang[3], Zhigang Ji[1], Ru Huang[3]
[1]Shanghai Jiao Tong University, [2]Peking University, Shenzhen, [3]Peking University, [4]Liverpool John Moores University

In this paper, a new physical-based model for flicker noise in advanced FinFET technology is proposed based on separation of intertwined noise sources. The proposed separation method can well clarify the sources of flicker noise, enabling the modeling of different components independently. The accuracy of this model is validated by the full-scale bias and size dependencies of flicker noise, as well as its variations. It is observed that ignoring noise sources other than oxide traps can result in an underestimation of approximately 60% under operating condition. The new model is readily to be used with commercial simulators for circuit-level analysis.

9:55 AM

32-3 Unveiling the Impact of High Frequency On-State and Off-State Operation on Gate Dielectric Reliability: A Comprehensive Analysis

Yu-Kai Chang[1], Pei-Chun Liao[1], You Sheng Liu[1], Pin-Shiang Chen[1], Ben Sou[1], Chih-Hua Wang[1], Ting Jui Huang[1], Wen-Hsien Chuang[1], Jen-Hao Lee[1]
[1]TSMC

In this work, on-state and off-state bias time-dependent dielectric breakdown are studied across DC to AC to mimic real circuit operation. For the first time, investigation of lifetime difference between AC square to sinusoidal waveform is reported. An oxygen vacancy-based simulation model is developed to describe dynamic defect evolution.

10:45 AM

32-4 Reversing a decades-long scaling law of dielectric breakdown for ReRAM forming voltage reduction - Modeling competition among defect generation and annihilation processes (Invited)

Ernest Y. Wu[1], Takashi Ando[1], Paul Jamison[1]
[1]IBM Research

In this work, we present and review a physics-based statistical model recently developed for our experimental findings of the *reverse* BD area scaling using hydrogen-plasma-treated HfO2 ReRAM devices, demonstrating no fundamental reason preventing the old scaling law from being reversed or altered, thus providing a solution for ReRAM technology scaling.

11:10 AM
32-5 <1ppm Device to Chip Level Reliability Characterization for High-Density DDR5 DRAMs
Namhyun Lee[1], Seonhaeng Lee[1], Gang-jun Kim[1], Youngjun Kim[1], Byoungwook Woo[2], Young-yun Lee[1], Hakgyun Kim[1], Eunjeong Kim[1], Yunsung Lee[1], Yuchul Hwang[2], Seungbum Ko[1], Sangwoo Pae[1]
[1]Samsung, [2]Samsung Electronics

An effective methodology of predicting the failure rates <0.01ppm using DRAM chips in one wafer was produced. Unlike previous methods that predict the statistical distribution with hundreds of test structures, $>10^8$ samples at the transistor level were measured for the first time, and the result follows weibull clustering model.

11:35 AM
32-6 A 256 Kbit $Hf_{0.5}Zr_{0.5}O_2$-based FeRAM Chip with Scaled Film Thickness (sub-8nm), Low Thermal Budget (350℃), 100% Initial Chip Yield, Low Power Consumption (0.7 pJ/bit at 2V write voltage), and Prominent Endurance (>10^{12})
Pengfei Jiang[1], Haijun Jiang[2], Yang Yang[1], Lu Tai[3], Wei Wei[1], Tiancheng Gong[1], Yuan Wang[1], Pan Xu[1], Shuxian Lv[1], Boping Wang[1], Jianfeng Gao[1], Junfeng Li[1], Jun Luo[1], Jianguo Yang[1,2], Qing Luo[1], Ming Liu[1,4]
[1]Institute of Microelectronics of Chinese Academy of Sciences, [2]Zhangjiang Lab, [3]School of Information Science and Engineering, Shandong University, Qingdao, China, [4]Fudan University

In this work, we successfully resolve the remanent polarization (P_r) degradation issue, which is caused by the thermal budget decreasing and the film thickness scaling of $Hf_{0.5}Zr_{0.5}O_2$ (HZO), and co-integrate the TiN/HZO/TiN capacitors with large initial P_r and low operating voltage in the Back-End-of -Line (BEOL) of 130nm CMOS technology to provide a 256kbit 1T1C FeRAM chip. The chip demonstrates 100% initial chip yield, >150mV sense margin after 10^{12} write cycles, power consumption of 0.7 pJ/bit at 2V write voltage, over 10^{12} endurance and 10 years retention.

Session 33: Sensors, Mems, and Bioelectronics (SMB) - In-Sensor Computing Systems
9:00 AM, Continental 6
Co-Chairs: Man Wong, HKUST and Sheng-Shian Li, National Tsing Hua University

This session includes 5 papers that describe the recent advances of in-sensor computing systems. In the first paper is presented 1-phototransistor-1-threshold switching optoelectronic neuron arrays that can directly sense, compress, encode, and interpret sensory data with ultra-low energy consumption, high recognition accuracy, and nearly zero accuracy loss based on the spiking neuron network. In the second paper is demonstrated a 3-tier integration of laser annealed crystallized Si CMOS circuit, BEOL 2T0C IGZO DRAM-like, and BEOL high photo-gain monolayer MoS2 phototransistor array on a single 8” Si wafer, thus offering a process platform capability of making sensors, circuits, and in-memory computing for smart image sensing systems. In the third paper is reported reconfigurable organic-inorganic hetero-transistors capable of ultrasensitive dim-light sensing and efficient in-sensor convolutional processing. In the fourth paper is reported an efficient point-of-care testing system based on memristor chip, which can support edge computing and realize real-time recognition of medical graphics with an error correction and in-situ recovery module. In the last paper is proposed an electronic nose that transforms raw sensor data into refined low-dimensional data for gas identification using an integrated gas sensor-amplifier merged array and in-memory computing block.

9:00 AM

33-1 1-Phototransistor-1-Threshold Switching Optoelectronic Neuron for In-Sensor Compression via Spiking Neuron Network

Rui Wang[1], Fanfan Li[2], Dingwei Li[2], Chuanqing Wang[2], Yingjie Tang[2], Guolei Liu[2], Saisai Wang[1], Yong Xie[1], Mohamad Sawan[2], Xiaohua Ma[1], Bowen Zhu[2], Min Qiu[2], Hong Wang[1], Yue Hao[1]
[1]Xidian University, [2]Westlake University

In this work, we demonstrate a 1-Phototransistor-1-Threshold Switching (1PT1TS) optoelectronic neuron with an In_2O_3 PT and NbO_x TS device for continuous-time in-sensor compression paradigm, which can directly sense, compress, encode, and interpret sensory data with ultra-low energy consumption and high recognition accuracy based on the spiking neuron network.

9:30 AM

33-2 3D Monolithically Integrated Device of Si CMOS Logic, IGZO DRAM-like, and 2D MoS_2 Phototransistor for Smart Image Sensing

Feng-Min Lee[1], Po-Hao Tseng[1], Yu-Yu Lin[1], Yu-Hsuan Lin[1], Wei-Lung Weng[1], Nei-Chih Lin[2], Po-Jung Sung[2], Chih-Chao Yang[2], Wen-Fa Wu[2], Chang-Hong Shen[2], Po-Han Chen[3], Yi-Hsien Lee[3], Ming-Hsiu Lee[1], Keh-Chung Wang[1], Chih-Yuan Lu[1]
[1]Macronix International Co., Ltd., [2]Taiwan Semiconductor Research Institute, [3]National Tsing Hua University

We proposed a M3D integration technology and constructed a unique platform to enable smart image sensor. This sensor includes 1st tier's 20nm Si FinFETs, 2nd tier's IGZO DRAM-like devices, and the top layer's 5x5 array of MoS_2 TMD phototransistors. All the functional units were fabricated for parallel image signal processing.

9:55 AM

33-3 Ultrasensitive Retinomorphic Dim-Light Vision with In-Sensor Convolutional Processing Based on Reconfigurable Perovskite-Bi_2O_2Se Heterotransistors

Lei Xu[1], Junling Liu[1], Shuo Liu[1], Liangliang Zhang[1], Ming He[1], Ru Huang[1]
[1]Peking University

Reconfigurable photosensors with superior bipolar optoelectronic performances based on the $MAPbI_3$-Bi_2O_2Se heterostructure were experimentally demonstrated for the first time. Analogue MAC operations such as Gaussian, Laplacian, and Inverse operators were successfully implemented in the reconfigurable photosensors, which exhibited outstanding performances on edge in-sensor image processing under dim-light scenes.

10:20 AM

33-4 Point-of-Care Testing (POCT) System based on self-Recovery Memoristor Chip with Low Energy Consuption(1.547 TOPS/W) and High Recognition (1142 fram/s)

Xu Zheng[1,2], Lizhou Wu[3], Yixuan Liu[3], Qiqiao Wu[3], Yuanlu Xie[1], Yi Li[1], Jinru Lai[1,4], Wenxuan Sun[1,2], Danian Dong[1,2], Jie Yu[5], Wenchang Zhang[1], Xiaoxin Xu[1], Ming Liu[1]
[1]Institute of Microelectronics of the Chinese Academy of Sciences, [2]University of the Chinese Academy of Sciences, [3]School of Microelectronics, Fudan University, [4]University of Science and Technology of China, [5]Fudan University

The Point-of-Care Testing (POCT) system based on image analysis suffers high power consumption, detection delay and lack of privacy security. In this work, we proposed an efficient POCT system based on memristor chip, which can support edge computing and realize real-time recognition of medical graphics. To solve the problem of the decrease of long-term inference accuracy caused by chip degradation, we designed the error correction and in-situ recovery module, which increased the recognition accuracy to 90% after 250 days. Benefit by the high speed and low power consumption of the memristor, the efficiency of POCT system is up to 1.547TOPS/W and the recognition rate is reach to 1142 frames/s.

10:45 AM

33-5 New Gas Identification Method Using Gas Sensor-Amplifier Merged Array and In-Memory Computing-Based Preprocessing

Gyuweon Jung[1], Jaehyeon Kim[1], Yujeong Jeong[1], Jinwoo Park[1], Wonjun Shin[1], Woo Young Choi[1], Jong-Ho Lee[1]
[1]Seoul National University

We present a novel gas identification method using a sensor-amplifier merged array and in-memory computing-based preprocessing. The sensing signals are preprocessed in the AND-type nonvolatile memory array and converted into refined data. Owing to well-refined data specific to the gas type, the system can accurately identify gas type and concentrations.

Session 34: Power, Microwave/Mm-Wave and Analog Devices/Systems (PMA) - High Frequency and Cryogenic RF Devices

9:00 AM, Continental 7-9
Co-Chairs: Troy Olsson, University of Pennsylvania and Pascal Chevalier, STMicroelectronics

This session includes 6 papers that describe either methods for scaling to devices to higher frequency or optimization for operation at cryogenic temperatures. The first paper by Zheng and Zhang of the Shanghai Institute of Microsystem and Information Technology details high performance lithium niobate on silicon carbide surface acoustic wave filters operating in the 5G NR and WiFi 6 bands. The second paper, by Garros from CEA-Leti, presents a drain extended SOI MOS transistor for applications in mm-wave PAs. The first of three papers on cryogenic electronics is given by Berlingard from CEA-Leti and the Univ. Grenoble Alpes and details back biasing methods to optimize performance of FD-SOI transistors at cryogenic temperatures. Jeong from KAIST gives a detailed treatment of the impact of channel thickness on the subthreshold swing of InGaAs HEMT targeted for cryogenic LNAs. Cha from IBM presents on the optimization of InGaAS HEMT ohmic contact resistance at cryogenic temperatures. Finally, Arabhavi from ETH Zurich details the THz characterization of InP/GaAsSb DHBTs demonstrating 1.46 THz fmax at 50K.

9:05 AM

34-1 Miniaturized Dual-Mode SAW Filters using 6-inch $LiNbO_3$-on-SiC for 5G NR and WiFi 6

Pengcheng Zheng[1,2], Shibin Zhang[1], Jin-xu Xu[3], Xiaoli Fang[1,2], Yang Chen[1,2], Kai Huang[1], Dongchen Sui[1,2], Xiuyin Zhang[3], Xin Ou[1,2]
[1]Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, [2]University of Chinese Academy of Sciences, [3]School of Microelectronics, South China University of Technology

Low-loss and wide-band SAW filters in the range of 3.3 to 6.3 GHz were demonstrated on 6-inch X-cut $LiNbO_3$-on-SiC. Further, the dual band SAW filters were demonstrated for the first time within compact footprints. The results show the potential of the dual-mode SAW technology using $LiNbO_3$-on-SiC for miniaturized and low-cost front ends.

9:30 AM

34-2 A cost effective RF-SOI Drain Extended MOS transistor featuring P_{SAT}=19dBm @28GHz & V_{DD}=3V for 5G Power Amplifier application

Xavier Garros[1,1], Alexis Divay[2], Joris Lacord[1], Ayssar Serhan[1], Thibaud Fache[1], Jasmina Antonijevic[3], Sébastien Crémer[3], Vincent Knopik[3], Alexandre Giry[4], Ismael Charlet[4], Rihab Chouk[5], Anne-Sophie Royet[1], Jérémie Forest[3], Nathalie Revil[3], Philippe Cathelin[3], Pascal Chevalier[3], David Roy[3], Fred Gaillard[1], Blandine Duriez[1]
[1]CEA-Leti, Univ. Grenoble Alpes, [2]CEA-Leti, Univ. Grenoble Alpes, France, [3]STMicroelectronics, [4]CEA Leti, Univ. Grenoble Alpes, [5]CEA-Leti, Univ. Grenoble Alpes

A high voltage N-type Drain Extended MOS (NDEMOS) in 40nm RFSOI technology is presented for PA application. NDEMOS PA cells exhibit 19.2dBm of P_{SAT}@V_{DD}=3V. With this NDEMOS device, this 300mm SOIMMW technology becomes a very cost-effective platform for Front End modules (FEM)

9:55 AM

34-3 RF performance enhancement of 28nm FD-SOI transistors down to cryogenic temperature using back biasing

Quentin Berlingard[1,2], Jose Lugo-Alvarez[1], Maryline Bawedin[2], Vincent Puyal[1], Flavio Bergamaschi[1], Mikaël Cassé[1]
[1]CEA-Leti, [2]IMEP-LAHC

We investigate back-gate bias impact on FD-SOI transistor behavior down to 4.2K, and demonstrate its advantage on RF performances of transistors and circuits for cryoCMOS. Characterizations are presented providing insights on the underlying physics. We defined optimization guidelines and applied it to a Low Noise Amplifier for operation at 4.2K.

10:20 AM

34-4 Impact of the channel thickness fluctuation on the subthreshold swing of InGaAs HEMTs at cryogenic temperature down to 4 K for ultra-low power LNAs

Jaeyong Jeong[1], Jongmin Kim[2], Jisung Lee[3], Yoon-Je Suh[1], Nahyun Rheem[1], Seong Kwang Kim[1,1], Juhyuk Park[1], Bong Ho Kim[1], Joon Pyo Kim[1], Seung-Young Park[3], Sanghyeon Kim[1]
[1]KAIST, [2]KANC, [3]KBSI

In this work, for the first time, we present and analyze the saturation mechanism in cryogenic InGaAs HEMTs. A novel interpretation of the phenomenon is proposed, predicated on the disorder resulting from potential fluctuations in the channel, attributable to the variability in channel thickness. We have discovered that the extent of potential fluctuation, induced by the fluctuation in channel thickness, differs according to the channel structure, which subsequently influences the degree of disorder. This understanding could lead to better design and operation of devices, particularly in the field of LNA for quantum computing.

11:10 AM

34-5 Cryogenic InGaAs HEMTs with Reduced On-Resistance using Strained Ohmic Contacts

Eunjung Cha[1], Alberto Ferraris[1], Peter Mueller[1], Hung-Chi Han[2], Daniele Caimi[1], Marilyne Sousa[1], Christian Enz[2], Cezar Bogdan Zota[1]
[1]IBM Research Europe, [2]Swiss Federal institute of Technology Lausanne (EPFL)

We have demonstrated InGaAs HEMTs with cryo-optimized tensile strained Ohmic contacts, for low-power qubit readout. The HEMTs achieved a record-low value of R_C of 30.6 Ω·μm, R_{ON} of 290 Ω·μm, and the noise indication factor, $\sqrt{I_{DS}}/g_m$, of 0.18 √Vmm/S, at the lowest power consumption reported in cryogenic low-noise HEMTs.

11:35 AM

34-6 THz InP/GaAsSb DHBTs with Record f_{AVG}=800 GHz: Characterization to 330 GHz

Akshay Kumar Mahadev Arabhavi[1], Marina Deng[2], Filippo Ciabattini[1], Sara Hamzeloui[1], Tamara Saranovac[1], Rimjhim Chaudhary[1], Mojtaba Ebrahimi[1], Olivier Ostinelli[1], Cristell Maneux[2], Colombo Bolognesi[1]
[1]ETH Zurich, [2]University of Bordeaux

We report the first independent characterization of THz "Emitter-Fin" double heterojunction bipolar transistors (DHBTs) up to 330GHz. An f_T/f_{MAX}=0.53/1.21THz was achieved, corresponding to a record $f_{AVG}=(f_T/f_{MAX})^{0.5}$=800GHz for HBTs. Further, we show cryogenic characterization of a THz-HBT with a record f_T/f_{MAX}=0.57/1.46THz at 50K for a 1.84 μm^2 DHBT.

Session 35: Memory Technology (MT) - Charge-Based Memories

1:30 PM, Grand Ballroom A
Co-Chairs: Maarten Rosmeulen, IMEC and Wanki Kim, Samsung

This session includes 7 papers on the topic of charge-based memories. The first invited paper discusses the status and novel ways to achieve >1000 layers in 3D NAND Flash. The second paper describes a high-performance 3D Flash memory based on CMOS Directly Bonded to Array (CBA). The third paper presents a

new read-retry scheme to reduce bit error rates in NAND Flash memories. The next two papers discuss advantageous charge trapping effects in ferro-electric FETs. The subsequent paper employs modeling to address plasma induced damage in NAND Flash technologies. The last paper provides a comprehensive study of NBTI and off-state reliability in DRAM technology.

1:35 PM
35-1 Fundamental Issues in VNAND Integration Toward More Than 1K Layers (Invited)
Jeehoon Han[1]
[1]Samsung Electronics

In a vertical NAND (VNAND) integration, which has the characteristic of increasing height, several major problems caused by height will be pointed out, and general approaches so far to solve them and new directions for the future will be presented.

2:00 PM
35-2 High Peformance 3D Flash Memory with 3.2Gbps Interface and 205MB/s Program Throughput based on CBA(CMOS Directly Bonded to Array) Technology
Shigeki Kobayashi[1], Kenji Tashiro[1], Youichi Minemura[1], Kohei Nakagami[1], Koji Arita[1], Takashi Oohashi[1], Kota Funayama[2], Hisaya Sakai[2], Mitsuteru Mushiga[2], Kenichi Okabe[2], Yoshihiro Kanno[2], Satoshi Shimizu[2], Eiichi Fujikura[2], Akihiro Nakae[2], Kensuke Yamaguchi[2], Hideyuki Yamawaki[1], Kazuaki Nakajima[1], Mitsuru Sato[1]
[1]Kioxia Corporation, [2]Western Digital Corporation

We report advantages of using CMOS directly bonded to array technology in 3D flash memory. Improvements in interface speed, operation latency, and memory cell reliability are explored based on experimental and simulated data from 218-word-line stacked structures. A chip architecture to achieve bit density of over 18Gb/mm^2 is also discussed.

2:25 PM
35-3 A Target-Read Retry Scheme for 3D Charge Trap NAND Flash Memory
You-Liang Chou[1], C.C. Lu[1], Wen-Jer Tsai[1], T.C. Lu[1], K.C. Chen[1], Chih-Yuan Lu[1]
[1]Macronix International Co., Ltd.
We propose a target-read retry (TRR) scheme to reduce bit error rate (BER) beyond the conventional read-retry method. A simple neighboring pattern recognition technique is disclosed due to the unique neighboring data pattern dependence of cells. 38% BER reduction and 3X retention time extension are achieved by the TRR scheme.

2:50 PM
35-4 Comprehensive Design Guidelines of Gate Stack for QLC and Highly Reliable Ferroelectric VNAND
Suhwan Lim[1], Taeyoung Kim[1], Ilho Myeong[1], Sanghyun Park[1], Suseong Noh[1], Seung Min Lee[1], Jongho Woo[1], Hanseung Ko[1], Youngji Noh[1], Moonkang Choi[1], Kiheun Lee[1], Sangwoo Han[1], Jongyeon Baek[1], Kijoon Kim[1], Juhyung Kim[1], Dongjin Jung[1], Kwangsoo Kim[1], Sijung Yoo[1], Hyun Jae Lee[1], Seung-Geol Nam[1], Ji-Sung Kim[1], Jaewoo Park[1], Chaeho Kim[1], Seunghyun Kim[1], Hyoseok Kim[1], Jinseong Heo[1], Kwangmin Park[1], Sanghun Jeon[2], Wanki Kim[1], Daewon Ha[1], Yu Gyun Shin[1], Jaihyuk Song[1]
[1]Samsung electronics, [2]KAIST

For the first time, a comprehensive guideline is proposed for a gate stack design of ferroelectric vertical NAND (Fe-VNAND), based on in-depth analytical modeling and experiments.

3:40 PM
35-5 High-Endurance FeFET with Metal-Doped Interfacial Layer for Controlled Charge Trapping and Stabilized Polarization

Kunifumi Suzuki[1], Kiwamu Sakuma[1], Yoko Yoshimura[1], Reika Ichihara[1], Kazuhiro Matsuo[1], Daisuke Hagishima[1], Makoto Fujiwara[1], Masumi Saitoh[1]
[1]Kioxia Corporation

We demonstrate the improvement of memory window (> 2V) and endurance (10^7 cycles) by controlling the interfacial trap charges in Si-channel HfO-FeFET. By introducing metal traps into the channel-side interfacial layer (IL), the IL degradation during cycling is suppressed, and the ferroelectric phase of HfO on the IL is stabilized.

4:05 PM
35-6 A Noble Design Methodology to Minimize Plasma Induced Damage Using a Distributed Network Model in VNAND Flash Memory
Se Hoon Lee[1], Junghwan Um[1], Kanglib Kim[1], Kyoungseo Lee[1], Seongpil Chang[1], Jaeshin Lee[1], Hunhee Han[1], Sungil Cho[1], Junhee Lim[1], Minchul Park[1], Sunghoi Hur[1]
[1]Samsung Electronics Co.

In this study, we successfully explained the By-pass Via(BVia) burnt phenomenon in VNAND Flash memory. We also proposed a novel methodology to optimize BVia arrangement using a distributed resistor network model, which resulted in damage-free BVia arrangement at the product level.

4:30 PM
35-7 Comprehensive Study of NBTI and Off-State Reliabilty in Sub-20 nm DRAM Technology: Trap Identification, Compact Aging Model, and Impact on Retention Degradation
Zixuan Sun[1], Puyang Cai[1], Jiahao Song[1], Da Wang[2], Zhuyou Liu[3], Longda Zhou[2], Tianxiang Zhu[1], Yongkang Xue[2], Yong Liu[2], Zirui Wang[1], Junwei Luo[3], Huixiong Deng[3], Yuan Wang[1], Zhigang Ji[2], Runsheng wang[1], Ru Huang[1]
[1]Peking University, [2]Shanghai Jiao Tong University, [3]Chinese Academic of Science

For the first time, we clarify the origin of NBTI traps in thick gate oxide HKMG DRAM peripheral transistors by determining their energy levels and relaxation energy distributions. Meanwhile, we systematically study OSD of DRAM for the first time in HKMG devices, presenting a different degradation result from SiON devices, and propose a new OSD mechanism. We develop compact aging models from trap-based approach that can accurately predict degradation and facilitate decoupling analysis of aging components. Finally, we discuss the impact of Sub Wordline Driver (SWD) aging on retention degradation.

Session 36: Neuromorphic Computing (NC) - Novel Computing Accelerators
1:30 PM, Grand Ballroom B
Co-Chairs: Vineet Agrawal, Infineon and Sapan Agarwal, Sandia

This session showcases cutting edge research to create novel computing accelerators. We start with an innovative approach to solving sparse regularized linear regression using $HfWO_x/VO_y$ based neurons. Next, we see an array level demonstration of a closed-loop circuit to accelerate the solution of problems with high complexity, such as matrix inversion with typical O(N^3) complexity with O(1) time. Subsequently, we will see how novel devices can be used to implement squared Euclidean distance for clustering and then how ternary multipliers can be used for computing polynomial functions. Finally, we hear about an innovative approach to solving optimization problems based on content addressable memory.

1:35 PM
36-1 An Ultrafast (< 200 ns) Sparse Solution Solver made by $HfWO_x/VO_y$ Threshold Tunable Neurons
Zirui Chen[1], Yue Zhou[2], Hanxi Xu[1], Yaoyao Fu[1], Yi Li[1,3], Yuhui He[4], Daniele Ielmini[5], Xiangshui Miao[1]
[1]Huazhong University of Science and Technology, [2]Department of Applied Physics, The Hong Kong Polytechnic University, Kowloon, Hong Kong, China, [3]Hubei Yangtze Memory Laboratories, [4]School of Integrated Circuits, Huazhong University of Science and Technology, [5]Politecnico Milano

A threshold tunable (V_{th}) neural component based on $HfWO_x/VO_y$ compound-layer memristor was developed showing ultra-fast device switching speed (～30ns) and based on it a one-step sparse solution solver was constructed with solution time <200ns for linear regression problems, which is 10^4 faster than CMOS ASIC scheme.

2:00 PM
36-2 An SRAM-based reconfigurable analog in-memory computing circuit for solving linear algebra problems
Piergiulio Mannocci[1], Enrico Melacarne[1], Andrea Pezzoli[1], Giacomo Pedretti[2], Corrado Villa[1], Flavio Sancandi[1], Umberto Spagnolini[1], Daniele Ielmini[1]
[1]Politecnico di Milano, [2]Hewlett Packard Labs

Closed-loop analog in-memory computing (AIMC) has attracted strong interest to accelerate solution of high-complexity problems by overcoming the memory wall. This work presents a reconfigurable AIMC-testchip capable of solving inverse problems with O(1) time. The circuit is experimentally validated on two real-world applications, namely massive multiple-input multiple-output and Kalman filter.

2:50 PM
36-3 Power-Efficient Clustering Using Programmable V_T FETs in Neuromorphic Architectures
Siddharth Barve[1], Nicholas Haehn[1], Connor Socolik[1,1], Aaron Ruen[1], Joshua Mayersky[1], Amber Reed[2,2], Kevin Leedy[2], Rashmi Jha[1]
[1]University of Cincinnati, [2]Air Force Research Laboratory

Existing Deep Neural Network (DNNs) implementations exceed power and time budgets of many applications. Additionally, DNN accelerators are supervised, highly specialized, and focus on multiply-and-accumulate operations. This work proposes a novel ultra-fast low power unsupervised neuromorphic architecture integrating programmable threshold voltage transistors for clustering using squared Euclidean distance.

3:15 PM
36-4 Hybrid-Domain In-Memory Polynomial Acceleration based on 40nm RRAM Multi-Core Chip for Machine Vision Calibration
Lin Bao[1,2], Zongwei Wang[1], Qishen Wang[1], Yuhang Yang[1], Yi Gao[1], Linbo Shan[1], Jingwei Sun[1], Yunfan Yang[1], Haisu Zhang[1], Cuimei Wang[1], Han Xiao[1], Le Ye[1], Ao Guo[3], Ling Shen[3], Wenbing Gu[3], Gaoming Feng[3], Chen Li[3], Shoumian Chen[3], Yuhang Zhao[3], Shanguo Huang[2], Yimao Cai[1], Ru Huang[1]
[1]Peking University, [2]Beijing University of Posts and Telecommunications, [3]ICRD

A novel hybrid-domain in-memory polynomial computing is proposed and experimentally demonstrated using 40nm RRAM chip with 30 integrated four-quadrant ternary multiplier arrays to realize high-order parallel polynomial matrix-vector computation, demonstrating software-comparable calibration of lens distortion with high calibration throughput (158Mpixels/s) and energy-efficiency (3.81Gpixels/W).

3:40 PM
36-5 Zeroth and higher-order logic with content addressable memories (Invited)
Giacomo Pedretti[1], Fabian Böhm[1], Mohammad Hizzani[2], Tinish Bhattacharya[3], Pedro Bruel[1], John Moon[1], Sergey Serebryakov[1], Dmitri Strukov[3], John Paul Strachan[2], Jim Ignowski[1], Thomas Van Vaerenbergh[1], Ray Beausoleil[1], Masoud Mohseni[1]
[1]Hewlett Packard Labs, [2]Peter Grünberg Institut (PGI-14) and RWTH Aachen University, [3]UC Santa Barbara

We demonstrate how to use Content Addressable Memories (CAMs) for asserting and solving zeroth order and higher-order logic. We demonstrate a ~6.5× lower area and ~4× lower energy per search and up to 175× faster time-to-solution for problems with 150 variables compared with memristor based Hopfield Neural Networks.

Session 37: Advanced Logic Technology (ALT) - Alternative Devices

1:30 PM, Continental 1-3
Co-Chairs: Xiuling Li, UT Austin and Paul Grudowski, NXP

This session highlights recent advances in alternative CMOS devices, including BEOL-compatible Amorphous Oxide Semiconductors (AOS) and Si Tunnel FETs for ultra-low-leakage. The first paper from National Yang Ming Chiao Tung University demonstrates an ultra-thin InSnZnO channel with 66.4mV/dec SS and low DIBL of 22mV/V. The second paper from Purdue reports record-low contact resistance to the In2O3 transistor by manipulating the charge neutrality level in Ni contacts. In the third paper from Georgia Tech, W-doped indium oxide (IWO) power FET BEOL compatibility is demonstrated for use in Heterogeneous 3D ICs. The next paper from Peking University reports record high drive currents along with low SS of 66mV/dec in gate-all-around IGZO nanosheet transistors. The last AOS paper in the session from Purdue focuses on thermal resistance and thermal capacitance scaling with channel length of In2O3 transistors. The final paper from Southeast University demonstrates a tunnel FET CMOS integration on a 300mm foundry platform for ultra-low-leakage MCU applications.

1:35 PM
37-1 First Demonstration of Highly Scaled Atomic Layer Deposited Ultrathin InSnZnO Channel Thin Film Transistor Exhibiting Superior Electrical Characteristics
Yan-Kui Liang[1], Jun-Yang Zheng[1], Yu-Lon Lin[1], Yu Chen[1], Kuan-Lun Chen[1], Dong-Ru Hsieh[1], Li-Chi Peng[1], Ching-Hua Chiu[1], Yu-Cheng Lu[1], Tsung-Te Chou[2], Chi-Chung Kei[2], Chun-Chieh Lu[3], Huai-Ying Huang[3], Yu-Ming Lin[3], Yuan-Chieh Tseng[1], Tien-Sheng Chao[1], Edward Yi Chang[1], Chun-Hsiung Lin[1]
[1]National Yang Ming Chiao Tung University, [2]Taiwan Instrument Research Institute, [3]Taiwan Semiconductor Manufacturing Company

For the first time, we successfully demonstrated scaled AOS TFTs featuring ultrathin 1.8 nm-thick ALD-deposited a-ITZO channel. The a-$In_{0.83}Sn_{0.11}Zn_{0.06}O$ TFT with L_{ch}= 40 nm stands out with a remarkably low DIBL value of 22 mV/V and a low SS of 66.4 mV/dec, surpassing most reported performances of quaternary AOS TFTs.

2:00 PM
37-2 Record-Low Metal to Semiconductor Contact Resistance in Atomic-Layer-Deposited In_2O_3 TFTs Reaching the Quantum Limit
Chang Niu[1], Zehao Lin[1], Zhuocheng Zhang[1], Pukun Tan[1], Mengwei Si[1], Zhongxia Shang[1], Yizhi Zhang[1], Haiyan Wang[1], Peide D Ye[1]
[1]Purdue university

We demonstrate the record-low metal-to-semiconductor contact resistance R_c=23.4Ωμm at n_{2D}=5.0×$10^{13}$$cm^{-2}$ (reaching the quantum limit) in atomic-layer-deposited In_2O_3 thin-film-transistors with back-end-of-line (BEOL) compatibility, enabled by the interfacial donor-like-trap-induced negative Schottky barrier. The ultra-low contact resistivity (ρ_c=1.3×10^{-9}Ωcm^2) and current-transfer-length (LT=2nm) position In_2O_3 as a highly promising candidate for ultra-scaled, high-performance BEOL transistors.

2:25 PM
37-3 BEOL Compatible Oxide Power Transistors for On-Chip Voltage Conversion in Heterogenous 3D (H3D) Integrated Circuits
Sunbin Deng[1], Jungyoun Kwak[1], Junmo Lee[1], Khandker Akif Aabrar[1], Tae-Hyeon Kim[1], Sharadindugopal Kirtania[1], Gihun Choe[1], Chengyang Zhang[1], Wantong Li[1], Omkar Phadke[1], Shimeng Yu[1], Suman Datta[1]
[1]Georgia Institute of Technology

To support vertical power delivery network in H3D stacked system, we developed high-voltage BEOL compatible IWO power transistors and superlattice capacitors. Based on our device technologies, simulated BEOL DC-DC converter allowed efficient voltage conversion in a multi-tier H3D transformer accelerator with multi-domains: logic (0.75V), eDRAM (1.5V) and FeFET (3V).

3:15 PM

37-4 First Demonstration of Sequential Integration for Stacked Gate-All-Around a-IGZO Nanosheet Transistors with Record I_d = 2.05 mA/&[mu]m, g_m = 1.13 mS/&[mu]m and Ultralow SS = 66 mV/dec

Qijun Li[1,2], Wenjie Zhao[2], Qianlan Hu[1], Chengru Gu[2], Shenwu Zhu[1,2], Honggang Liu[2], Ru Huang[1], Yanqing Wu[1]
[1]Peking University, [2]Huazhong University of Science and Technology

We provide first demonstration of high-performance stacked gate-all-around (GAA) a-IGZO nanosheet field-effect transistors (NSFET). A record-high g_m of 1.13 mS/μm at V_{ds} =1.5 V, ultralow SS of 66 mV/dec and record-high on-state current of 2.05 mA/μm at V_{ds} =1 V are demonstrated with excellent on/off ratio > 10^{11}.

3:40 PM

37-5 First Determination of Thermal Resistance and Thermal Capacitance of Atomic-Layer-Deposited In_2O_3 Transistors

Jian-Yu Lin[1], Zhuocheng Zhang[1], Sami Alajlouni[1], Pai-Ying Liao[1], Zehao Lin[1], Chang Niu[1], Ali Shakouri[1], Peide D Ye[1]
[1]Purdue University

In this work, we determined the thermal resistance (R_{TH}) and the thermal capacitance (C_{TH}) of atomic-layer-deposited In_2O_3 field-effect transistors for the first time using a thermo-reflectance imaging system. Through the extracted R_{TH} and C_{TH}, the heat dissipation capability of In_2O_3 transistors is found to be related to the device geometry.

4:05 PM

37-6 A Sub-100nA Ultra-low Leakage MCU Embedding Always-on Domain Hybrid Tunnel FET-CMOS on 300mm Foundry Platform

Yaoru Hou[1], Kaifeng Wang[2], Chenxing Liu-Sun[1], Jianfeng Hang[2], Xinfang Tong[1], Chunyu Peng[3], Yongqin Wu[4], Ye Ren[4], Weihai Bu[4], Xin Si[1], Bo Liu[1], Xiulong Wu[3], Jun Yang[1], Hao Cai[1], Qianqian Huang[2], Ru Huang[2]
[1]Southeast University, [2]Peking University, [3]Anhui University, [4]Semiconductor Technology Innovation Center (Beijing) Corporation

This work firstly demonstrates a microcontroller-unit (MCU) based on 55nm TFET-CMOS hybrid 300mm foundry platform. By utilizing the record high I_{ON}/I_{OFF} ratio of the dopant segregation TFET, a 1Kbit TFET-SRAM is implemented in MCU always-on domain. Experimental results show that TGG-SRAM and TFET-MCU obtain order of magnitude standby power reduction.

Session 38: Power, Microwave/Mm-Wave and Analog Devices/Systems (PMA) - Wide Bandgap Devices for Power and RF Applications

1:30 PM, Continental 4
Co-Chairs: Cezar Zota, IBM and Andrei Vescan, RWTH Aachen

This session covers recent developments in wide bandgap materials for RF and high-frequency power applications. The first paper from Xidian University sets a new benchmark for power density at X- and Ka-band with 33.1 W/mm and 14.6 W/mm respectively achieved with 150 nm gate length AlGaN/GaN HEMTs on SiC substrates. Moving to 200mm diameter Si substrates, CEA Leti presents optimized AlN/GaN MISHEMT with an in-situ SiN gate dielectric showing impressive 6.6 W/mm at 26GHz with a PAE of 41.1%. The immense promise of this device structure is confirmed by the equally impressive results originating from imec, with ft/fmax of 80 GHz/190 GHz achieved with 200nm gate length devices and excellent power performance. This is followed by Xidian University with a b-Ga2O3 RF MOSFET on SiC substrate with 30% power-added efficiency and ft/fmax of 27.6/57 GHz. Next, a millimeter-wave GaN impact ionization avalanche transit-time diode oscillator operating at Ka-band is demonstrated by Stanford. Finally, the session concludes with an invited paper by Prof. Mohammad Samizadeh Nikoo from ETH Zürich on a novel metadevice concept based on microscopic manipulation of RF electric fields, with applications within future telecommunication technologies.

1:35 PM

38-1 Record Power Performance of 33.1 W/mm with 62.9% PAE at X-band and 14.4 W/mm at Ka-band from AlGaN/GaN/AlN:Fe Heterostucture

Ling Yang[1], Fuchun Jia[1], Hao Lu[1], Bin Hou[1], Meng Zhang[1], Jiale Du[1], Qingyuan Chang[1], Longge Deng[1], Qian Yu[1], Shiming Li[1], Mei Wu[1], Xiaohua Ma[1], Yue Hao[1]
[1]Xidian University

In this work, we present ultra-high power performance achieved by AlGaN/GaN/AlN:Fe device at X- and Ka-band. The device achieved record P_{out} of 33.1 W/mm and peak PAE of 62.9% at 10 GHz for power and PAE-tuned. The scaled-down device delivers a maximum P_{out} up to 14.4 W/mm at 30 GHz.

2:00 PM

38-2 High Performance mmWave AlN/GaN MISHEMTs on 200 mm Si Substrate

Sachin Yadav[1], Alireza Alian[1], Rana ElKashlan[1,2], Barry J O'Sullivan[3], Ahmad Khaled[1], Babak Kazemi Esfeh[1], Uthayasankaran Peralagu[1], Sourish Banerjee[1], Bertrand Parvais[1,2], Nadine Collaert[1]
[1]imec, [2]VUB, [3]IMEC

We demonstrate high performance AlN/GaN MISHEMTs on 200 mm Si substrate grown using MOCVD. We systematically studied the trade-off between RF small- and large-signal performance on scaling AlN and in-situ SiN gate dielectric thicknesses. A record large-signal performance at 28 GHz is achieved.

2:25 PM

38-3 6.6W/mm 200mm CMOS compatible AlN/GaN/Si MIS-HEMT with in-situ SiN gate dielectric and low temperature ohmic contacts

Erwan Morvan[1], Yveline Gobil[1], Fanny Morisot[1], Jérôme Biscarrat[1], Matthew Charles[1], Jose Lugo[1], Alexis Divay[1], Mohammed Medbouhi[1], Ismael Charlet[1], Julien Delprato[1], Pascal Scheiblin[1], Bledion Rrustemi[1], Alexandre Giry[1], Ayssar Serhan[1], Simon Ruel[1], Patricia Pimenta-Barros[1], Fabien Laulagnet[1], Stephane Minoret[1], Arnaud Anotta[1], Thierry Billon[1], Blandine Duriez[1]
[1]CEA Leti

Development of 200mm CMOS compatible SiN/AlN/GaN/Si MIS-HEMT process for Ka-band PAs with soft gate process, in-situ SiN gate dielectric, low temperature ohmic contacts, low RF losses and GaN:C back-barrier. 2x50µm devices with Lg=150nm show Ft/F_{MAX} of 81/173GHz and competitive performance with GaN/SiC at V_{DD}=20V with PAE/PSAT =41%/6.6W/mm at 28 GHz.

2:50 PM

38-4 1.1 A/mm &[beta]-Ga_2O_3-on-SiC RF MOSFETs with 2.3 W/mm P_{out} and 30% PAE at 2 GHz and f_T/f_{max} of 27.6/57 GHz

Min Zhou[1], Hong Zhou[1], Sen Huang[2], Mengwei Si[3], Yuhao Zhang[4], Tiantian Luan[2], hongqing Yue[1], kui dang[1], chenlu wang[1], zhihong liu[1], Jincheng Zhang[1], Yue Hao[1]
[1]Xidian University, [2]Institute of Microelectronics of Chinese Academy of Sciences, [3]Shanghai Jiao Tong University, [4]Virginia Polytechnic Institute and State University

This work innovatively combines the β-Ga_2O_3-on-SiC material platform, highly-doped β-Ga_2O_3 channel, and a T-gate with field plate, which allows for a concurrent realization of high $I_{D,max}$=1.1A/mm, high f_T/f_{max}=27.6/57GHz, CW P_{out}/PAE= 2.3W/mm/30%@2 GHz, 1.5W/mm/25%@3 GHz, 1.3W/mm/17%@5 GHz and 0.7 W/mm/7%@8 GHz, setting several new records in β-Ga_2O_3 RF power transistors.

3:40 PM

38-5 Demonstration of Millimeter-Wave GaN IMPATT Oscillator at Ka-band

Zhengliang Bian[1], Avery Marshall[2], Cheng Pao[2], Tracy Lee[2], Srabanti Chowdhury[1]
[1]Stanford University, [2]QuinStar Inc

A GaN IMPATT oscillator operated at Ka-band is demonstrated for the first time.The diodes adopted a single-drift-region p^+-n structure grown on native GaN substrates. A beveled mesa etch with SiO_2 sidewall passivation

enabled robust avalanche breakdown and high current capabilities in the devices. To minimize the series resistance, the substrate was thinned down to 100 μm. The avalanche was preserved in the diodes after the substrate thinning. RF oscillation characterization was performed in a microstrip cavity circuit. An oscillation up to 38.0 GHz was achieved at a biasing current density of 10.2 kA/cm^2 with a peak output power of 7 dBm.

4:05 PM

38-6 High-Performance GaN Electronic Metadevices: Towards 6G Telecommunications (Invited)

Mohammad Samizadeh Nikoo[1], Boce Lin[1], Yuqi Liu[1], Hua Wang[1]
[1]School of Information Technology and Electrical Engineering, ETH Zürich

Electronic metadevice is a new concept in which microscopic manipulation of radiofrequency fields results in exceptional device properties. We demonstrate critical experiments on high-speed GaN electronic metadevices, with cutoff frequency of 10 THz, which showcase their potential for future telecommunication circuits. We realized monolithically-integrated switches achieving low insertion-loss (~3 dB) and high isolation (~15 dB) at terahertz frequencies. A highly-linear operation at high-power densities above 6 W/mm with input-third order-intercept-point of 150 W/mm, was shown. We also demonstrate frequency-doublers with conversion gains approaching the theoretical limit of an ideal diode, and broad-band frequency up-conversion of 10-Gbps QPSK signals into mm-wave band.

Session 39: Emerging Device and Compute Technology (EDT) - BEOL Compatible Technologies

1:30 PM, Continental 5

Co-Chairs: Hyejung Choi, SK-Hynix and Tomonari Yamamoto, Tokyo Electron Ltd.

This session includes 6 papers that describe recent advances in BEOL compatible technologies for logic memory, BEOL transistors and RF devices. The first paper, by Shuhan Liu of Stanford University, guidelines for oxide semiconductor transistor co-designed for gain cell memory on the logic platform. The second paper, by T. Sriman of Stanford University (Invited), describes recent advances and challenges of their N3XT 3D Technology Foundations targeting 1,000× system-level Energy Delay Product benefit. The third paper, by S. Van Beek of imec, demonstrates a path towards maximizing efficiency in SOT-MRAM. The fourth paper, by H. Suhail of University of California, Los Angeles, demonstrates the first integration of the VC-MTJ device with CMOS and explored its array level performance. Through this demonstration, the potential of VC-MRAM / MeRAM as an upcoming high density and energy efficient embedded memory will also been shown. The fifth paper, by Xin Wang of Peking University, demonstrates high-performance monolayer WSe2 pFETs based on BEOL compatible growth and fabrication without transfer, providing a new pathway for 2D TMDC CMOS circuit with integration capability. The sixth paper, by Qianlan Hu of Peking University, demonstrates record high cut-off frequency up to 48 GHz in top-gate ITO transistors on SiC substrate proving the potential in highly reliable logic and radio-frequency applications toward 3D monolithic integration.

1:35 PM

39-1 Gain Cell Memory on Logic Platform – Device Guidelines for Oxide Semiconductor Transistor Materials Development

Shuhan Liu[1], H.-S. Philip Wong[1], Koustav Jana[1], Kasidit Toprasertpong[1], Jian Chen[1], Qi Jiang[1], Sumaiya Wahid[1], Shengjun Qin[1], Wei-Chen Chen[1], Zheng Liang[2]
[1]Stanford University, [2]University of California, Berkeley

This work starts with memory macro simulation and establishes guidelines for oxide-semiconductor(OS) transistor co-designed for gain-cell memory on the logic platform. ALD ITO FET is chosen to balance retention time with memory bandwidth. The experimentally optimized device has low off-current 2×10^{-18}A/μm, high on-current 26.8μA/μm. OS/hybrid gain-cell memory macro simulated using this optimized device operates at V_{DD}=0.9V, has 480,000×retention, 1.5×/4.1×frequency compared with Si gain-cell, and 0.5×/0.98×frequency of SRAM. Hybrid OS-Si gain-cell has 3×density of SRAM, and OS-OS gain-cell has N*1.15×density of SRAM with N-layer of 3D stacking. DNN simulation shows ~50% reduction in execution time due to larger on-chip memory capacity.

2:00 PM

39-2 *N3XT 3D* Technology Foundations and Their Lab-to-Fab: *Omni 3D Logic, Logic+Memory Ultra-Dense 3D, 3D Thermal Scaffolding* (Invited)

Subhasish Mitra[1], Tathagata Srimani[1], Andrew Denis Bechdolt[1], Suhyeong Choi[1], Carlo Gilardi[1], Anna Kasperovich[1], Shengman Li[1], Qing Lin[1], Mohamadali Malakoutian[1], Patrick James McEwen[1], Robert M Radway[1], Dennis T Rich[1], Andrew Yu[2], Sam Fuller[3], Sara Achour[1], Srabanti Chowdhury[1], H.-S. Philip Wong[1], Max Shulaker[2]
[1]Stanford University, [2]MIT, [3]Analog Devices

N3XT 3D is a disruptive computing systems technology targeting 1,000× system-level Energy Delay Product benefits for abundant-data applications such as AI/machine learning and graph analytics. We present *N3XT 3D* technology foundations, recent advances and challenges, and successful lab-to-fab transition to industrial facilities.

2:25 PM

39-3 Scaling the SOT track – A path towards maximizing efficiency in SOT-MRAM

Simon Van Beek[1], Kaiming Cai[1], Farrukh Yasin[1,1], Hubert Hody[1], Giacomo Talmelli[2], Van Dai Nguyen[1], Anna Trovato[1], Nathali Franchina[1], Alvaro Palomino[1], Kurt Wostyn[1], Siddharth Rao[1], Gouri Sankar Kar[2], Sebastien Couet[1]
[1]imec, [2]IMEC

We demonstrate the functionality of an extreme perpendicular spin-orbit torque (SOT)-MRAM where the SOT layer and magnetic tunnel junction (MTJ) pillar exhibits comparable dimensions. This novel design leads to a significant reduction in the power consumption (63% decrease), an enhancement in endurance (>10^{15} cycles), and a reduction in bit-cell area.

3:15 PM

39-4 The First CMOS-Integrated Voltage-Controlled MRAM with 0.7ns Switching Time

Haris Suhail[1], Haoran He[1], Jiyue Yang[1], Qingyuan Shu[1], Chih-Yao Wang[2], Shan-Yi Yang[2], Yu-Chen Hsin[2], Cheng-Yi Shih[2], Hsin-Han Lee[2], Di Wu[1], Albert Lee[1], Jeng-Hua Wei[2], Puneet Gupta[1], Kang L. Wang[1], Sudhakar Pamarti[1]
[1]University of California, Los Angeles, CA, USA, [2]Industrial Technology Research Institute, Hsinchu, Taiwan

In this paper, we present the first CMOS-integrated VC-MRAM. The VC-MRAM shows an ultra-fast 700ps switching time using 1.8V write voltage. The switching time has good uniformity, and 92% switching probability is achieved across the array. Reliability of >10^{11} write cycles and read time of 8.5ns are demonstrated.

3:40 PM

39-5 BEOL Compatible High-Performance Monolayer WSe_2pFETs with Record G_m=190 μS/μm and I_{on}=350 μA/μm by Direct-Growth on SiO_2 Substrate at Reduced Temperatures

Xin Wang[1,2], Xinhang Shi[2], Xiong Xiong[1], Ru Huang[1], Yanqing Wu[1]
[1]Peking University, [2]Huazhong University of Science and Technology

We reported the low temperature synthesis of monolayer p-type WSe_2 crystals directly on SiO_2 via non-local heating. Record-high g_m of 190 μS/μm and I_{on} of 350 μA/μm of the 100 nm pFET at V_{ds}=-1 V are demonstrated based on monolayer WSe_2 grown on 5 nm SiO_2 dielectric at 450 ℃.

4:05 PM

39-6 First Demonstration of Top-Gate Indium-Tin-Oxide RF Transistors with Record High Cut-off Frequency of 48 GHz, Id of 2.32 mA/ μm and gm of 900 μS/μm on SiC Substrate with Superior Reliability at 85 °C

Qianlan Hu[1], Chengru Gu[2], Shiyuan Liu[1], Min Zeng[2], Shenwu Zhu[2], Jiyang Kang[2], Ranhui Liu[2], Wenjie Zhao[2], Anyu Tong[1], Qijun Li[2], Tianyue Fu[1], Ru Huang[1], Yanqing Wu[1]
[1]Peking University, [2]Huazhong University of Science and Technology

We demonstrate high performance and high reliability ITO transistor on SiC substrate with record-high I_d of 2.32 mA/mm and g_m of 900 mS/mm at V_{ds} = 1 V at 85 °C. Record high f_T up to 48 GHz has also been achieved, the highest among all amorphous oxide semiconductor transistors.

Session 40: Optoelectronics, Displays, and Imaging Systems (ODI) - Image sensors
1:30 PM, Continental 6
Co-Chairs: Pierre Magnan, ISAE-Supaero and Jun Ogi, Sony Semiconductor Solutions

This session includes 6 papers describing the most recent advances in the field of Image Sensors. The first paper by Lee from Samsung Electronics describes a 0.5 μm pixel, 3 layers-stacked, CMOS Image Sensor (CIS) with in-pixel Cu-Cu bonding technology featuring improved conversion gain and noise. The two next papers present new achievements in the area of Voltage Domain Global Shutter (VDGS) CIS. In the second paper, Gao from Omnivision presents a 2.2 μm - 2 layer stacked High Dynamic Range VDGS CIS with 1x2 shared structure offering Dual Conversion Gain and achieving low FPN. In the third paper, Malinge from STMicroelectronics presents a 2.16 μm 6T BSI VDGS CIS using Deep Trench Capacitors and achieving 90 dB Dynamic range (DR) using spatially-split exposure. In the fourth paper, Berkovich from Meta presents a 2 Megapixel - 4.23 μm pixel pitch - offering block-parallel A/D architecture and featuring programmable sparse-capture with a fine grain gating scheme for power saving. The next paper, by Shirahige from Canon, introduces a new Twisted Photodiode CIS structure - 6 μm pixel pitch - enabling all-directional autofocus for high speed and accuracy and 95 dB DR. Finally Shan, from Shanghai Jiao Tong University, presents a 64x64 pixels organic imager prototype based on a novel hole transporting layer (HTL)-free structure achieving highest record low light performances.

1:35 PM
40-1 A 0.5μm Pixel 3-layer Stacked CMOS Image Sensor with Deep Contact and In-pixel Cu-Cu Bonding Technology

Gwi-Deok Ryan Lee[1,1], Dae-Hoon Kim[1], Doowon Kwon[1], Jong-Eun Park[1], Dongseok Cho[1], Jeongsoon Kang[1], Gyunha Park[1], Junha Kang[1], Minho Jang[1], Seungjae Oh[1], Doyeon Kim[1], Sol Yoon[1], Yongjun Kim[1], Sejin Park[1], Kyungtae Lim[1], Dongjun Oh[1], Sooyoung Kang[1], Keunhyoung Park[1], Changhwa Kim[1], Hyoju Kim[1], Taeyeong Kim[1], Kyu-Ha Lee[1], Hyoukyung Cho[1], Son-Kwan Hwang[1], Hojin Lee[1], Jae-kyu Lee[1], Hyunchul Kim[1], Chang-rok Moon[1], Jaihyuk Song[1]
[1]Samsung Electronics

64Mp CIS with 0.5um pixels has been developed with three wafer layers. The RTS noise was reduced by 85% compared to ones of the conventional structure with over 6,000e- FWC. The FD conversion gain was improved by 67% with the Miller effect due to the reduction of the DCNT capacitance.

2:00 PM
40-2 A 2.2μm 2-Layer Stacked HDR Voltage Domain Global Shutter CMOS Image Sensor with Dual Conversion Gain and 1.2e- FPN

Zhe Gao[1], Geunsook Park[1], Linda Fu[1], Genis Chapinal[1], Joseph Yang[1], Tom Freson[1], Qing Qin[1], Jiayu Guo[1], Fan Zhu[1], Shaomin Ding[1], Zhiqiang Lin[1], Alan Chih-Wei Hsiung[1], Keiji Mabuchi[1], Tomas Geurts[1], Lindsay A. Grant[1], T.J. Dai[1]
[1]OMNIVISION

The world's smallest HDR voltage-domain global shutter image sensor with 2.2μm pixel pitch was fabricated based on a 2-layer stacking process. This design features single exposure dual conversion gain capture, dual exposure capture and low noise performance, i.e. 1.2e-rms of pixel level fixed pattern noise and 3.8e-rms of temporal noise.

2:25 PM

40-3 2.16μm Back Side Illuminated Voltage Domain Global Shutter CMOS Image Sensor with single silicon layer pixel

Pierre Malinge[1], Frederic Lalanne[2], Didier Herault[2], Thomas Ferrotti[1], Laurent Simony[2], Stephanie Bigault[1], Julien Favreau[1], Thomas Nassiet[1], Yolene SACCHETTINI[1], Christine Augier[1], Stephane Ricq[1], Patrice Waltz[1], Florent Brun[1], Nicolas Roux[1], Arnaud Glais[1], Gregory Roffet[1], Lookah Chua[1], Jansen Reyes Duey[1], Arnaud Tournier
[1]STMicroelectronics, [2]STmicroelectronics

We present the smallest 2.16μm pitch voltage domain global shutter pixel built on a single silicon layer. A novel pixel architecture is used along a very dense front-end capacitor integration, leading to the smallest sensor size for the given 800x700 resolution, with high quantum efficiency and spatial resolution at 940nm.

3:15 PM

40-4 A 3D-Integrated 2-Megapixel Imager with Sparse Capture and Fine-Grain Power Gating

Andrew Berkovich[1], Shlomo Alkalay[1], Tsung-Hsun Tsai[1], Chiao Liu[1], Mika Laiho[2], Ari Paasio[2], Jonne Poikonen[2], Mika Grönroos[2], Mika Kutila[2], Petteri Mäki[2], Mika Naula[2], Tero Säntti[2], Tuomo Komulainen[2]
[1]Meta, [2]Kovilta Oy

We present a 3D integrated 2-megapixel image sensor with programmable sparse capture, fine grain power gating, and block-parallel ADC architecture. Several power gating mechanisms are combined to minimize energy and readout latency for specified sampling patterns. We demonstrate >7x reduction in frame energy and readout latency.

3:40 PM

40-5 Cross Dual-Pixel Twisted-Photodiode Image Sensor for All-Directional Auto Focus

Daiki Shirahige[1], Koichi Fukuda[1], Hajime Ikeda[1], Yusuke Onuki[1], Ginjiro Toyoguchi[1], Hiroshi Sekine[1], Shuhei Hayashi[1], Kohei Okamoto[1], Shunichi Wakashima[1], Ryo Yoshida[1], Junji Iwata[1], Yasushi Matsuno[1], Katsuhito Sakurai[1], Hiroshi Yuzurihara[1], Takeshi Ichikawa[1]
[1]Canon Inc.

We present a newly developed CMOS image sensor with high AF performance based on a twisted PD structure, in which the photodiode is twisted by 90 degrees. The proposed structure realizes PDAF at all pixels and in all directions, and the minimum AF illuminance level of 0.007 lux is achieved.

4:05 PM

40-6 Organic Active-Matrix Imager with Ultra-low Illumination Detection Capacity for Lens-Free Optical Analysis

Tong Shan[1], Jun Li[1], Chao Zhou[1], Fangyuan Chang[1], Xiaojun Guo[1]
[1]Shanghai Jiao Tong University

A novel structure of hole transporting layer-free is developed for organic photodiodes (OPDs), which effectively reduces the dark current and boosts the photocurrent simultaneously. An active-matrix imaging array prototype is developed with imaging capacity under ultra-low light intensity (4 nW cm^{-2}). Our demo shows versatile applicability for lens-free optical analysis.

Session 41: Reliability Of Systems and Devices (RSD) - Reliability of TFT and GaN Devices

1:30 PM, Continental 7-9

Co-Chairs: William Vandendaele, CEA-Leti and Inanc Meric, Intel

This session covers "Reliability of TFT and GaN transistors" and consists of six papers, four focusing on Semiconductor Oxide TFT reliability and two on GaN HEMT reliability and thermal management. The first paper on TFT reliability shows the reduction of BTI and an improved Ion/Ioff ratio on InGaO-based TFT using Fluorine doping. The second paper of the session presents a novel ITO-IGZO bilayer channel using DG (Double Gate) integration that improves immunity to PBS/NBS degradation and enables low thermal budget IGZO FeFET processing. The third paper proposes a combined use of DG operation and W-doping to mitigate BTI and HCD effects in In2O3 based TFTs. The final paper on TFT devices investigates the IGZO channel thickness influence on LFN and BTI degradation. The next two papers address new findings on GaN HEMTs reliability. The fifth paper of the session presents an understanding of the lateral ON-state breakdown in GaN HEMT based on charge redistribution in the back-barrier. The final paper highlights measurement and modeling of thermal management in GaN HEMTs by optimized utilization of multi-finger configuration.

1:35 PM

41-1 Fluorine Anion-Doped Ultra-Thin InGaO Transistors Overcoming Mobility-Stability Trade-off

Jie Zhang[1,2], Zhuocheng Zhang[1], Hongyi Dou[1], Zehao Lin[1], Ke Xu[1], Weifeng Yang[2], Xinghang Zhang[1], Haiyan Wang[1], Peide D Ye[1]
[1]Purdue university, [2]Xiamen University

We report the first demonstration of BEOL-compatible ultra-thin (~3 nm) fluorine-doped InGaO TFTs with Lch down to 60 nm, achieving E-mode operation with highest Ion/Ioff and remarkably high degree of thermal and bias stability. This study provides a new research direction of overcoming mobility-stability trade-off by anion-doping techniques.

2:00 PM

41-2 Negative-U Defect Passivation in Oxide-Semiconductor by Channel Defect Self Compensation Effect to Achieve Low Bias Stress V_{TH} Instability of Low-Thermal Budget IGZO TFT and FeFETs

Chun-Kuei Chen[1], Zefeng Xu[1], Sonu Hooda[1], Jieming Pan[1], Evgeny Zamburg[1], Aaron Voon-Yew Thean[1]
[1]National University of Singapore

Here, we elucidate the fundamental reliability mechanism in oxide-semiconductor to improve interface/bulk-induced V_{TH} degradation. We provide insights into the ITO-IGZO channel defect-self compensation effect to passivate channel negative-U defects effectively. Our DG ITO-IGZO devices achieved a record-low NBS/PNS V_{TH} shift of 30mV, a 10x NBS/PBS improvement against the mono-IGZO devices.

2:25 PM

41-3 Improved Reliability and Enhanced Performance in BEOL Compatible W-doped In_2O_3 Dual-Gate Transistor

Khandker Akif Aabrar[1], Sharadindugopal Kirtania[1], Sunbin Deng[1], Gihun Choe[1], Asif Islam Khan[1], Shimeng Yu[1], Suman Datta[1]
[1]Georgia Institute of Technology

We investigate both hot carrier induced degradation (HCD) and positive bias stress instability (PBTI) in back-end-of-the-line (BEOL) compatible tungsten-doped In_2O_3 (IWO) dual-gate field effect transistor (DG-FET) with scaled-EOT(1.18nm) gate stack. The DG-FET shows simultaneous improvement in threshold voltage (V_T) stability and enhancement in device performance. The DG-FET exhibits 11mV V_T-shift under 4.24 MV/cm oxide field ($E_{ox}=V_{overdrive}/EOT$) stress for 1Ks, while exhibiting drive current gain of 3x over the back-gate (BG) FET. This makes the IWO DG-FET a viable BEOL transistor candidate for enabling next generation monolithic 3D (M3D) ICs.

3:15 PM

41-4 Unveiling the Influence of Channel Thickness on PBTI and LFN in Sub-10 nm-thick IGZO FETs: A Holistic Perspective for Advancing Oxide Semiconductor Devices

Gan Liu[1], Qiwen Kong[2], Xiaolin Wang[3], Yi-Hsin Tu[1], Zijie Zheng[3], Chen Sun[1], Dong Zhang[1], Yuye Kang[1], Kaizhen Han[3], Gengchiau Liang[1], Xiao Gong[1]
[1]National University of Singapore, [2]National University of Singapore, [3]National University of Singapore

In this work, we present the first systematic and comprehensive investigation into the impact of channel thickness (t_{CH}) on the positive bias temperature instability (PBTI) and low frequency noise (LFN) of Indium-Gallium-Zinc-oxide (IGZO) FETs with sub-10 nm t_{CH}. This work highlights the significance of adopting a holistic approach to understanding and optimizing device performance in advancing oxide semiconductor device technology.

3:40 PM
41-5 Charge Movement in Back Barrier Induced Time-Dependent On-State Breakdown of GaN HEMT
Hao Yu[1], Jingtian Fang[2], Bjorn Vermeersch[1], Uthayasankaran Peralagu[1], Han Han[1], Olivier Richard[1], Alireza Alian[1], Nelson de Almeida Braga[2], Babak Kazemi Esfeh[1], Sourish Banerjee[1], Erik Bury[1], Bertrand Parvais[1,3], Nadine Collaert[1]
[1]imec, [2]Synopsys, [3]VUB

We elucidate a mechanism behind time-dependent on-state breakdown of GaN HEMTs, where the time-to-failure varies from sub-μs to hundreds of seconds. We reveal that the breakdown is sequentially caused by charge movement in the back barrier (BB), drain-corner electric field densification, impact ionization, and avalanche breakdown.

4:05 PM
41-6 Thermal Management in Multi Finger GaN on Si HEMTs: Understanding and Mitigating Self Heating and Thermal Crosstalk for Enhanced Device Reliability, Jaeyong Jeong[1], Sung Joon Choi[1], Joonsup Shim[1], Eunjung Kim[1], Seong Kwang Kim[1], Bong Ho Kim[1], Joon Pyo Kim[1], Yoon-Je Suh[1], Woo Jin Beak[1], Dae-Myeong Geum[2], Yumin Koh[3], Donghyun Kim[3], Sanghyeon Kim[1]
[1]KAIST, [2]Chungbuk National University, [3]KANC

This study examines thermal mechanisms in single and multi-finger GaN-on-Si HEMTs, using high-resolution thermoreflectance microscopy. We find multi-finger device reliability differs from single-finger ones and identify the unique reliability degradation mechanism for multi-finger GaN-on-Si HEMTs. To address thermal crosstalk, we propose a novel non-uniform multi-finger configuration and validate its enhanced reliability. These insights could help overcome performance and reliability issues caused by thermal effects in various power and GaN devices.

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